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Speed, Power Efficiency, and Noise Improvements for Switched Capacitor Voltage Converters

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by

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Switched-capacitor (SC) DC-DC converters provide a viable solution for on-chip DC-DC conversion as all the components required are available in most processes. However, power efficiency, power density characteristics of SC converters are adversely affected by the integration, and characteristics such as response time and noise can be further improved with an on-chip converter. An analysis on speed, power efficiency, and noise performance of SC converters is presented and verified using simulations. Based on the analysis two techniques, converter-gating and adaptive gain control, are developed. Converter-gating uses a combination of smaller stages and reconfiguration during transient load steps to improve the power efficiency and transient response speed. The stages of the converter are also distributed across the die to reduce the voltage drop and noise on power supply. Adaptive gain control improves transient response through manipulation of the gain of the integrator in the control loop. This technique focuses on improving the response time during converter reconfiguration and offers a general solution to transient response improvement instead of focusing on the worst case scenario which is usually the largest transient load step. The techniques developed are then implemented in ST 28nm FDSOI process and test methodologies are discussed.

CHAPTER 1:

INTRODUCTION

As the demand for high performance electronics in industrial, military and consumer markets is growing, wide variety of solutions are designed and developed. These solutions, regardless of the requirements they fulfill, always need a power management and delivery system as they all rely on a power supply that behaves within specific limitations. For example, a data conversion circuit used in high precision data conversion may require a power supply that has very low voltage ripple around a constant voltage, or a microprocessor may require a power supply that can change its output voltage for dynamic voltage scaling (DVS). So, invariably all the electronic solutions require a power management and delivery system to a certain degree even if it is something as simple as a carefully designed metal lines or as complex as a DVS system. This requirement makes the research in power management and delivery very valuable as the power section of a circuit usually determines the maximum achievable performance.

With the scaling of integrated circuits, however, the power delivery is becoming the bottleneck for performance [1, 2]. Because the integrated circuit operating voltages scale down with the advancements in processing technology while the battery and external power source voltages remain relatively constant. This fact, combined with the increased power consumption of the integrated circuits put stringent requirements on power management and delivery systems since now a higher conversion ratio is needed and a higher amount of current needs to be delivered. The two aspects of the power delivery problem therefore is addressed using two approaches, i) by implementing high efficiency, high conversion ratio DC-DC converters to reduce the losses during voltage conversion and to reduce the current requirement, ii) by employing methods such as DVS at the load side to reduce the total power needed by the load circuit and by optimizing the on-chip power delivery. These

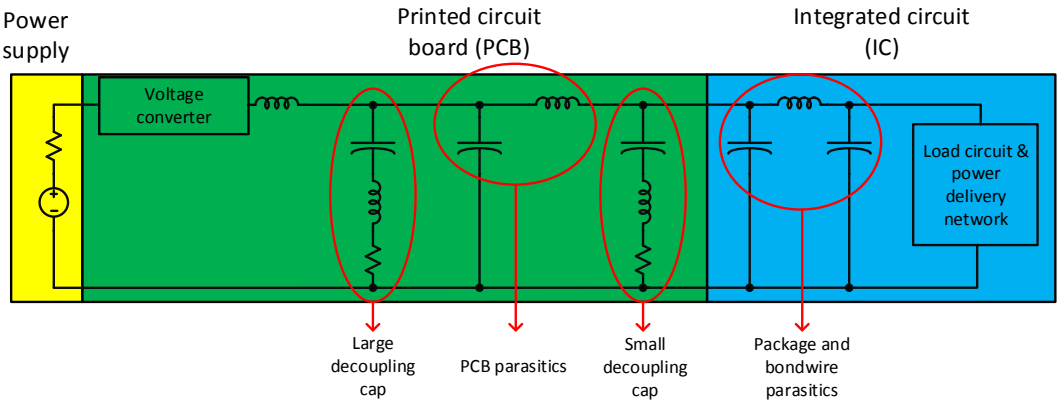


Figure 1.1: Off-chip voltage conversion and regulation offer highly efficient and flexible solution but the parasitics in between the voltage converter and the load circuit may cause problems for systems with stringent requirements.

two approaches can be implemented together using a single DC-DC converter that has configurable output voltage level for DVS and a high conversion ratio.

Conventionally DC-DC conversion and the power management and delivery is implemented outside the load circuit using discrete elements or dedicated integrated circuits as shown in Fig. 1.1. In the system shown, the voltage converter is implemented as a separate element on the printed circuit board (PCB) and once the voltage is converted to a usable voltage for the load and regulated it is given to the load circuit which is an integrated circuit. Although this system offers a very easily scalable and high efficiency solution, the PCB and IC package parasitics may limit the performance. For example, often two decoupling capacitors with different values are placed on the PCB to act as a reservoir and respond to the load transients quickly. However, even if the decoupling capacitors can be placed next to the IC, the package parasitics still limit the fastest response and if the parasitics between the voltage converter and the decoupling is large enough, voltage converter may not be able to replenish the charge lost from the capacitors fast enough to maintain a constant voltage, introducing higher noise and drop on the power supply. Moreover, the power reduction features such as DVS rely heavily on being able to change the voltage levels of the power supply in short amount of time. With an external voltage converter, the amount of time required to change the power supply voltage is limited by the PCB parasitics and the decoupling capacitors.

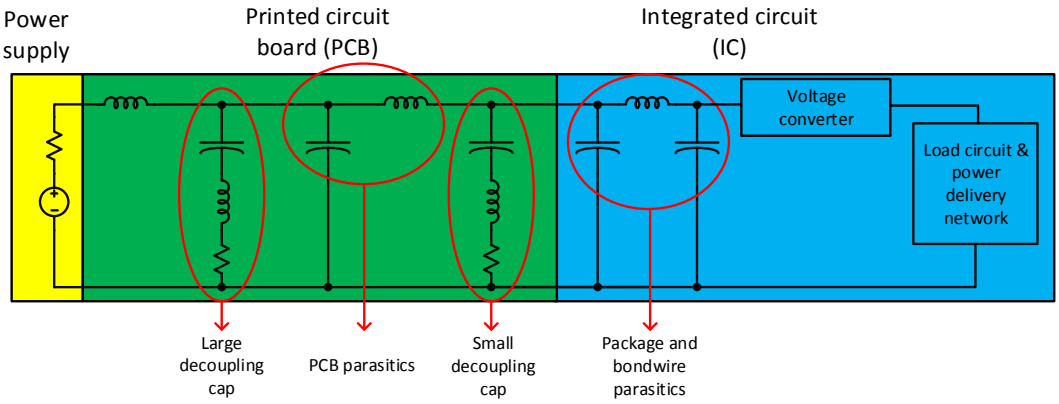


Figure 1.2: On-chip voltage conversion and regulation is more challenging as the energy storage elements such as inductors and capacitors are harder to implement on-chip but on-chip system bypasses all the parasitics.

The shortcomings of an external power delivery and management system can be overcome by integrating the voltage converter and power delivery system into the IC. Such a system is shown in Fig. 1.2. With on-chip voltage converters and power delivery, all the parasitics of the PCB can be bypassed and the load power supply voltage can be regulated within a loop that is much closer to the load. Having lower parasitics on the power delivery path can help with simplifying PCB design requirements, while the on-chip voltage regulation loop can help achieving very fast voltage level shifting. Moreover, an on-chip voltage conversion scheme greatly reduces the PCB footprint which is important in mobile applications where the physical size is very limited.

As a result, the on-chip voltage conversion is becoming common for power delivery and management solutions. There are different architectures that can be used to implement on-chip voltage converters, so the merits of the on-chip voltage converters and comparison of commonly used architectures will be discussed next.

1.1 On-Chip Voltage Converters

To enable complete on-chip power conversion and delivery, it is necessary to reduce the total occupied area of these devices while still maintaining high power efficiency. The total area occupied by the voltage converter is important as it is directly related to the total manufacturing cost of

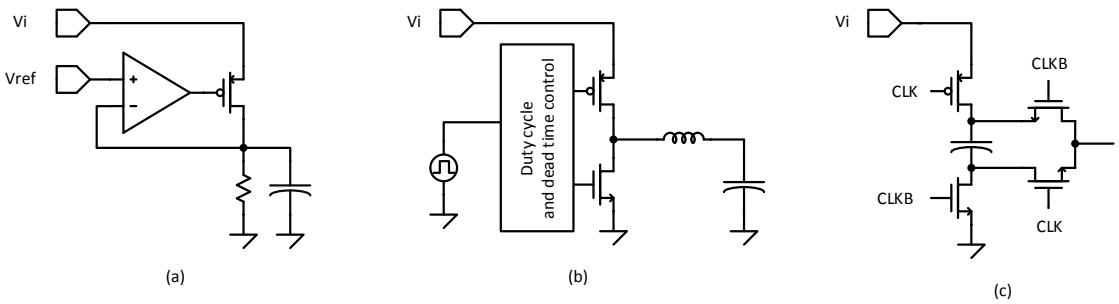


Figure 1.3: Comparison of commonly used on-chip voltage converters a) low dropout regulator b) buck converter c) switched capacitor converter.

the die, it is also important to keep the load as close to the voltage converter as possible. On-chip components usually have lower efficiency since the processes are usually optimized for the operation of the transistors and not for the passive devices such as capacitors and inductors. As it will be explained later, these two objectives are often conflict, therefore the performance of on-chip voltage converters is usually determined by their power density (W/mm^2) and power efficiency (%)

In modern devices, on-chip voltage converters are usually implemented using three dominant topologies. These topologies are low dropout regulators (LDO), buck converters (inductance-based), switched capacitor converters (capacitance-based). There are also hybrid configurations available but these are out of the scope of this work [3]. The advantages and disadvantages of these converters are summarized in the next sections.

1.1.1 LDO Regulators

LDOs offer simplest and most widely used solution to the power delivery problem. An LDO includes a power transistor controlled by a feedback loop to stabilize its output voltage. This type of regulators provide, fast response as the feedback loop is usually only limited by the stable bandwidth of the error amplifier. The power to the output flows through the power transistor, and its power density is usually limited by the current density of transistors available in a given technology which is usually high enough to surpass the density of the other two topologies. Also because the output is usually controlled in a continuous time loop, these type of converters have clean output signals which does not include ripples and is limited by the noise performance of the

device. However this type of regulators suffer from large power efficiency drop as the difference between output and the input voltage gets higher. The reason behind this is the fact that the same current that is going to the output has to flow through the adjustable resistor which is the power transistor. This means that for every unit current that is delivered to the output at the voltage V_o has to come from the voltage supply V_i. Therefore the efficiency of the LDOs are ultimately limited by V_o/V_i ratio. Because of their efficiency limitation, LDOs reduce the benefits of using DVS, and are not suitable for high conversion ratios. LDOs however can be used to generate cleaner outputs from a noisy power supply, and are suitable for on-chip distribution because of their high power density [4–7].

1.1.2 Buck Converters

Buck converters are inductance based converters. In buck converters the current and direction of the current on an inductance is adjusted to create a specific output voltage. The conventional method of controlling the current flow through the inductance is using two power transistors, one connected to supply voltage and the other connected to ground. The switching activity in this configuration causes a varying current to go through the inductance, which in turn creates the output voltage. The switching activity causes output to have a certain amount of ripple voltage, causing spurs in the spectrum of the output voltage. Usually this type of converters are implemented in a duty cycle based control loop. Duty cycle determines the time spent during power transistor connected to the supply or the one that is connected to the ground. Controlling the duty cycle with enough resolution allows this type of converters to generate a wide range of output voltages. From efficiency perspective, the buck converter is efficient for the higher conversion ratios, as the power is not wasted on a resistor. Instead it is stored on the inductance and converted to another voltage. In an ideal buck converter, for every unit of current delivered to the load at half of the supply voltage requires only half unit of current as the inductance is used in the operation. However power efficiency of these converters are affected by the losses in the circuit and therefore is not 100 % except in ideal case. These losses include, parasitic losses of the inductance, switching losses and switch driving losses. State of the art buck converters are able to deliver high output power at high

efficiencies.Buck converters are suitable for DVS systems as output voltage range is large, and this type of converters provide high power density if not as high as LDOs. However the implementation of high quality inductances on-chip remains to be a problem even in modern technologies, inductors occupy a large area with large overhead (*i.e.* active area underneath is usually left unused) and are not very scalable meaning implementing many small inductors is not as area efficient as implementing a large inductor.

1.1.3 Switched Capacitor Voltage Converters

Switched capacitor voltage converters use capacitors in different configurations to deliver power to output. Usually this type of converters have a charging phase when the capacitors are charged to a pre-determined voltage level, and a discharging phase during which the charge stored on the capacitors are delivered to the output. Frequency of operation as well as the duty cycle can be and is being used in controlling the output voltage levels. However since capacitors charge to a certain voltage in a certain configuration, these converters usually have a single ideal conversion ratio at which they generate ideally 100 % efficiency. The output voltage can be changed using frequency and duty cycle but the efficiency for a single converter is ultimately limited by $V_o/(n \times V_i)$ where n is the conversion ratio for a specific configuration [8]. To overcome dependency of efficiency on topology, converters with multiple ratios are being used in literature. The power efficiency of these converters are again reduced by the losses which are parasitics of capacitors, switching losses and switch driving losses. State of the art SC converters are as efficient as inductive converters with comparable power densities [9]. This type of converters are suitable for DVS systems, and provide a medium range power density and benefit from the high quality and dense capacitors provided by the technology kit.

As summarized above three types of converters are main candidates for on-chip voltage conversion. In this work SC converters are chosen for following reasons, i) SC converters do not require implementation of elements that are not in baseline CMOS technology (advantage over buck converters) therefore easier to integrate on chip, ii) SC converters provide higher efficiencies

compared to LDOs and in par with the buck converters, iii) SC converters are optimum for low-medium output power with high efficiency and the power output is highly scalable.

1.2 Objectives

To enable on-chip voltage conversion using SC converters certain performance metrics of SC converters must be improved. First, power efficiencies comparable with external DC-DC converters have to be achieved at high power densities, because any degradation in power efficiency translates as increased power consumption which may hinder the benefits of using an on-chip voltage converter. Second, the advantages of on-chip converters must be exploited to improve the power supply integrity. Third, the transient response of the SC converters under different configurations or conditions must be improved for fast DVS applications and to reduce the power supply noise during load transients. Fourth, the developed methods should be proven using simulations and silicon implementation.

1.3 Organization

This work is organized as follows. In Chapter 2 the power efficiency is analyzed for SC converters and based on the analysis the converter-gating technique is introduced. This technique uses a combination of smaller SC converters to maintain high efficiency at lower output currents. Several other aspects of SC converters are also improved through using properties of the proposed method in Chapter 2.

In Chapter 3 the charge transfer in reconfigurable converters and converters with response enhancements is analyzed. Based on this analysis the implications of reconfiguration on transient response is discussed. The transient response of these converters are improved through using a new method which adaptively changes the gain of the integrator in the control loop.

In Chapter 4 the design procedure and the implementation details of a test chip in 28nm FDSOI technology is discussed. Each subcircuit is explained, test methodologies and future improvements are presented.

In Chapter 5 conclusions are drawn from the results and possible future work options are presented.

CHAPTER 2:

LEVERAGING ON-CHIP SC VOLTAGE REGULATORS TO IMPROVE HARDWARE SECURITY, TRANSIENT RESPONSE AND POWER SUPPLY INTEGRITY

2.1 Introduction

The continuous advancements in the semiconductor industry and transistors with smaller than 20 nm feature size have enabled the integration of multi-billion transistors on a single die [10, 11][1]. With the failure of Dennard's scaling [12], however, only a fraction of the transistors on a die can operate at full voltage/frequency in order not to exceed the thermal design power (TDP) [13, 14]. A large proportion of the circuit blocks is either inactive (dark silicon) or in a reduced-power state (dim silicon) at any given time to satisfy the power and thermal constraints [15, 16]. Despite the significant amount of research and growing necessity for a holistic power optimization technique, existing efforts to minimize power dissipation are typically not coherent, as highlighted in the report for the NSF Workshop on Cross-layer Power Optimization and Management (CPOM'12) [17]. The existing research efforts are disjointed into two pieces: i) the dynamic and static power loss at the load circuits is minimized or ii) the power loss during power-conversion is minimized.

Circuits typically enter reduced power states when the workload is light to save power and reduce the cost of cooling. On-chip voltage regulators, however, operate indifferently under varying workload conditions and generally provide optimum efficiency for a certain output power. Since dynamically changing the design parameters of a voltage regulator under different workloads

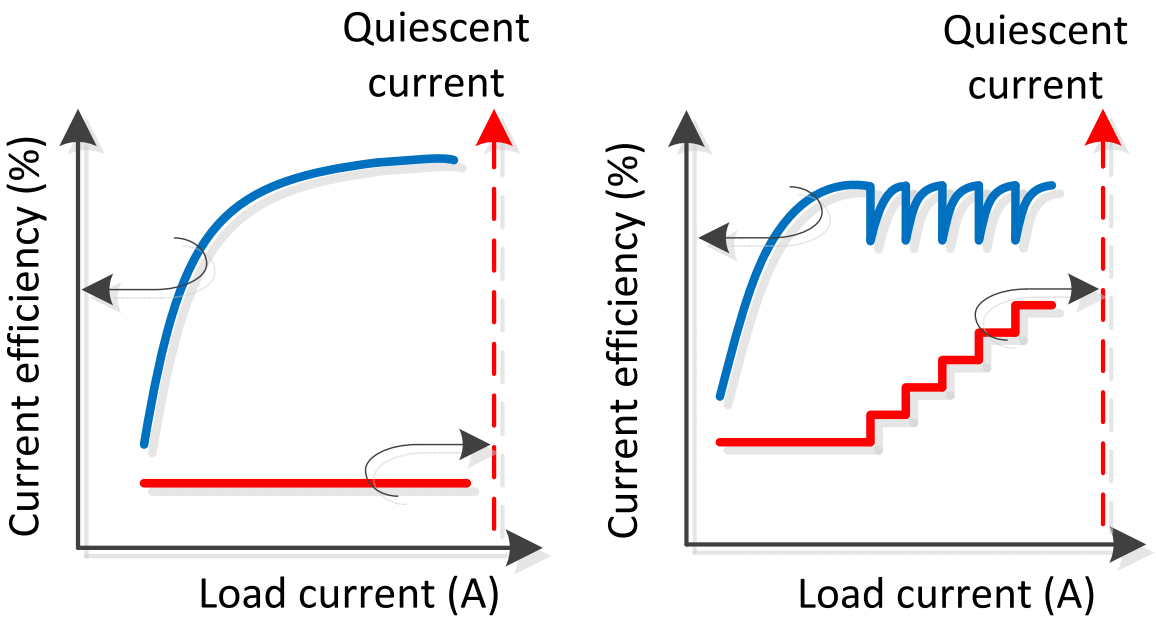
[1]This chapter was published in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 4, no. 2, pp. 169-179, June 2014 "Converter-Gating: A Power Efficient and Secure On-Chip Power Delivery System" and in 2014 IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, 2014, pp. 13-18 "Regulator-Gating Methodology with Distributed Switched Capacitor Voltage Converters". Permissions are included in Appendix B.

is difficult, existing power management techniques suffer from increased voltage conversion losses during idle states when the current demand is low [1, 18, 19].

Another growing concern is the security of the information that is processed or stored within ICs. Several techniques are used by attackers to obtain the secret information or functionality and a widely used non-invasive technique is the side channel power attacks. In these attacks, the correlation between the stored information (or functionality) and power consumption of the IC is exploited. Various input combinations are typically applied to the IC by an attacker. The correlation among the power consumption profiles for different input patterns is statistically analyzed to solve the secret key or learn the secret functionality [20]. Most of the side channel attacks can be mitigated if the internal power consumption is masked from the attacker by either: i) injecting excess current at certain times to obtain a quite constant power consumption profile [21] or ii) scrambling the on-chip power consumption to disrupt the correlation between the logic operations and power consumption profile [22]. These widely used techniques significantly degrade the overall efficiency of the power delivery system [23, 24]. In this chapter, specialized power management techniques are presented as a countermeasure to side channel power attacks without degrading the power efficiency of the system.

Below are the primary contributions presented in this chapter:

- A workload aware, secure converter-gating technique is proposed in this chapter. Individual stages within an interleaved switched capacitor (SC) voltage converter are turned on and off based on the load current demand.
- A configurable SC voltage converter circuit is proposed that provides $\sim$10$\times$ faster transient response as compared to the conventional SC converters.
- The amplitude of the output voltage ripple is reduced by utilizing the flying capacitors within deactivated converter stages as decoupling capacitors is proposed.
- An efficient countermeasure for side channel power attacks is proposed. The correlation between the internal logic operations and the overall chip power consumption is significantly disrupted with the proposed randomized converter-gating.



(a) (b)

Figure 2.1: Current efficiency of different LDO regulators. a) Current efficiency of an LDO regulator increases monotonically with the load current when the quiescent current is constant. b) Adaptively controlling the quiescent current based upon the load current can improve the current efficiency.

The related background and motivation for the proposed voltage regulator management technique is provided in the next section.

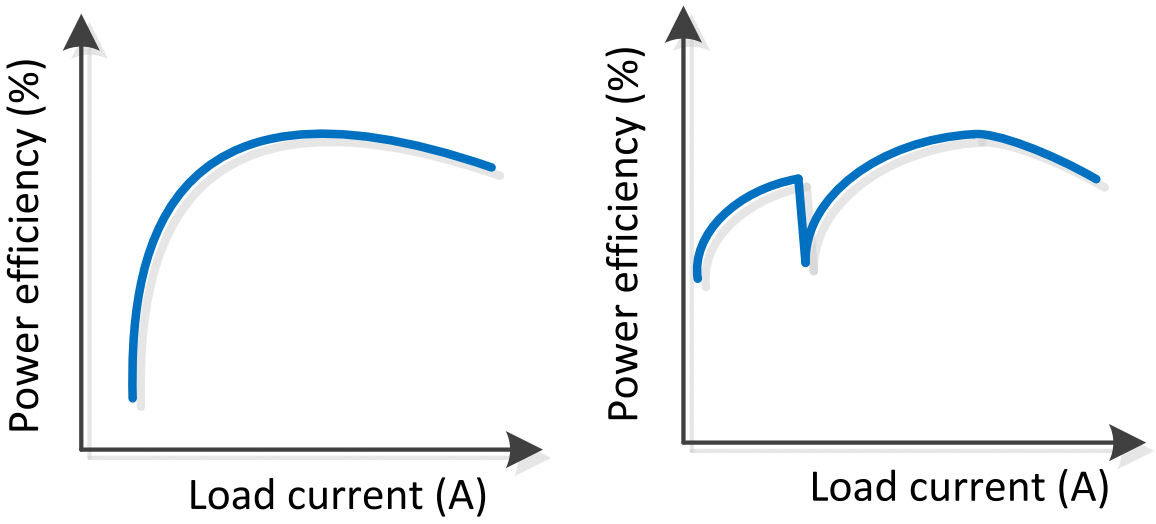
The proposed converter-gating technique is explained in Section 2.3. The circuit level design details are offered in Section 2.4. The proposed converter-gating technique is validated with extensive simulations in Section 2.5. The chapter is concluded in Section 2.6.

2.2 Background and Motivation

More than 32% of the overall power is dissipated during high-to-low voltage conversion before even reaching the load circuits in modern mobile platforms [25]. The primary reason for this huge power loss is that power delivery networks are designed to satisfy the stringent noise requirements under the *worst-case* loading conditions, which is typically the full utilization of the overall chip computing and memory resources when the current demand is the highest. The current or power efficiency of low-dropout (LDO) regulators, SC converters, and buck converters are illustrated in

Figs. 2.1, 2.2, and 2.3, respectively. The current efficiency of an LDO regulator depends on the quiescent current consumption. Although the efficiency of an LDO regulator can be improved by adaptively changing the quiescent current, current efficiency is significantly degraded at light load currents, as shown in Fig. 2.1b [5, 26]. The power conversion efficiency of a conventional SC converter increases with the output current and reduces significantly at light loads, as illustrated in Fig. 2.2a. Although advanced techniques are used to improve the power conversion efficiency at light load currents, as illustrated in Fig. 2.2b [27], the power conversion efficiency is typically degraded while providing light output current. The power conversion efficiency of a buck converter is also degraded significantly while delivering light load current, as shown in Fig. 2.3. All the on-chip voltage regulator topologies suffer from degraded power efficiencies while providing light output current. When the load circuit is in idle or sleeping mode, the voltage converter is driven into this low power conversion efficiency region, reducing the overall power conversion efficiency of power delivery system. Although significant power savings are achieved at the load circuits during reduced power states, these saving can be easily boosted if the power delivery system adaptively configures itself based on the workload under a wide range of load currents.

Another performance limiting factor in power delivery is the parasitic impedance of the power grid network between the voltage converter and load circuits. When the voltage regulator is implemented off-chip, the parasitic impedance of the off-chip interconnection networks and power/-ground pins degrade the power suply integrity by increasing the response time, and IR and Ldi/dt voltage drops. Many techniques, such as a flipped voltage (super source) follower [26] and adaptive bias current [28], have been proposed to enable on-chip implementation of LDO regulators. Even though LDO regulators provide fast response time, the power conversion efficiency of linear regulators is limited to $\frac{V_o}{V_{in}}$ where V_{in} and V_o are, respectively, the input and output voltages [29]. To obtain higher power conversion efficiency for a wide range of conversion ratios, the SC converters can be used, which are the main foci in this chapter. With the continuous technology scaling, high density on-chip capacitors can be realized on-chip. SC converters with high density on-chip capacitors can achieve 4.6 W/mm^2 power density, with ~86% efficiency [30].



(a) (b)

Figure 2.2: Power efficiency of different SC converters. a) The power efficiency of an SC converter is not necessarily monotonic but the maximum efficiency is typically obtained while delivering a certain output current. b) Different techniques can be used to improve the efficiency at light load currents.

Distributed voltage regulation has recently gained attention as this technique can provide fast transient response and low noise [31–36]. Parallel integration of LDO regulators can breed challenges such as device mismatch, offset voltages among parallel regulators, overall system stability, and balanced current sharing, however, distributed voltage regulation can provide sub-nanosecond load regulation to attain high performance under increased temporal and spatial workload variations in modern ICs. Bulzacchelli *et al.* achieved 500 ps transient response time with a system of eight distributed LDO regulators [33]. Alternatively, individual stages of an interleaved SC converter can be distributed throughout the power grid without the aforementioned challenges. In interleaved converters, each interleaved converter stage operates at a different phase of a clock signal to minimize the output voltage ripple [37, 38]. Interleaved converters reduces the filter size, provides higher power efficiency [39], and by distributing the interleaved stages, the power supply noise can be minimized.

On-chip voltage regulators can also be used as a countermeasure to side channel power attacks by preventing attackers to obtain the actual power consumption information [40–43]. A

constant overall power consumption profile can be obtained by inserting a certain amount of excess current in addition to the actual load current. The sum of the excess current and actual current consumed by the active circuit blocks is kept constant by scaling the excess current inversely proportional to the actual current [21]. The primary disadvantage of this technique is the huge power loss to maintain constant power consumption, especially when the load current demand is low. Another technique is to randomize the current provided to the chip from outside and disrupt the correlation between the overall power consumption and load current consumption. A power profile scrambling technique is proposed in [22] to change the amplitude and frequency of the input current spikes. All of these mitigation techniques increase the overall power consumption and therefore degrade the overall system performance.

An important motivation for this work is the observation of a strong impact of the type of the voltage regulator on the power consumption profile. LDO regulators are typically employed as on-chip voltage regulators. A primary problem of utilizing on-chip LDO regulators for secure applications is the direct relationship between the input and output current of an LDO. Due to this intrinsic characteristic, LDO regulators typically leak the maximum possible power consumption information to the attacker if no advanced techniques are employed to mask the power consumption.

Alternatively, in this work, a new switching regulator architecture is used to reduce the dependence of the input current on load current. When switching regulators are utilized, the input current is no longer linearly dependent on the load current. The correlation between the input current and load current is further reduced by reconfiguring the number of active phases within a switched capacitor converter with the proposed technique. Details of the proposed approach that ensures secure on-chip power delivery are explained in Section 2.4.4.

2.3 Converter-Gating

The details of the proposed converter-gating technique are explained in this section. The working principle of conventional SC converters and their power loss mechanisms are explained in Section 2.3.1. A case study that motivates the proposed work is explained in Section 2.3.2. The

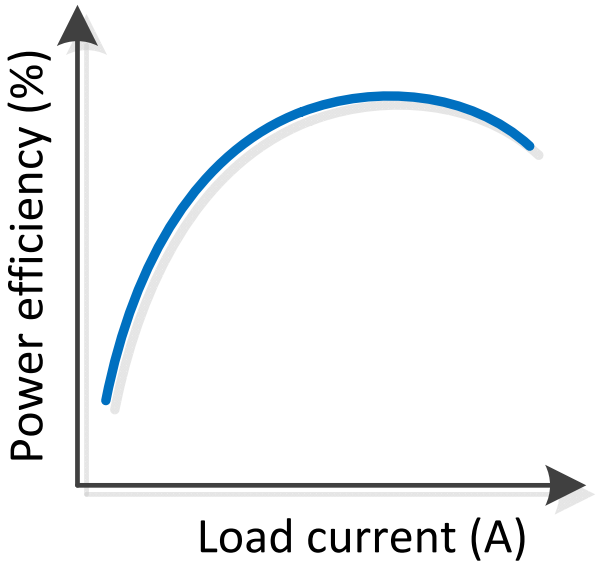


Figure 2.3: Power efficiency of buck converters. The efficiency graph exhibits a non-monotonic behavior and the maximum power efficiency is obtained at a certain output current.

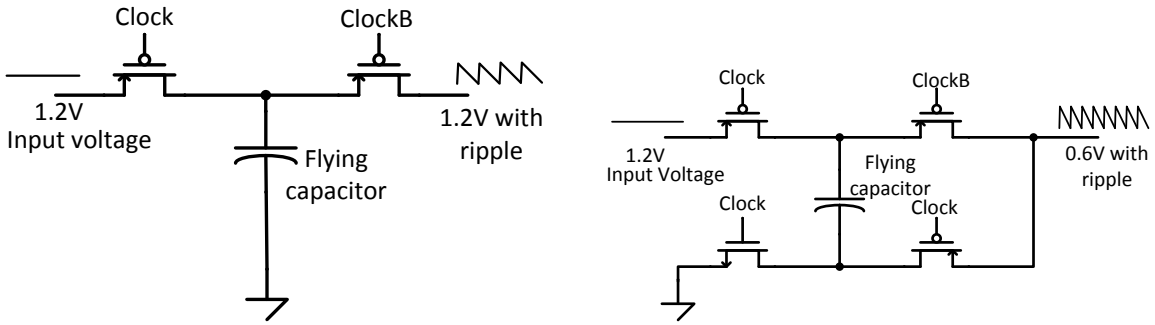


Figure 2.4: Two different topologies for SC voltage converters where the MOSFET switches are controlled with non-overlapping *Clock* and complimentary *ClockB* signals. a) 1:1 converter with two switches and a flying capacitor. b) 2:1 converter with four switches and a flying capacitor.

proposed control mechanism that adaptively turns on and off individual SC converter stages is discussed in Section 2.3.3.

2.3.1 Efficiency Analysis of Switched Capacitor Voltage Converters

A conventional SC voltage regulator is composed of multiple switches, a capacitor network, and related feedback circuits. A clock signal is used to control the switches through which the capacitors are charged to a certain voltage level based on the converter topology and pulse width of clock

period. Another group of switches, controlled by a complementary non-overlapping clock signal, connects the capacitor to the output node to deliver the stored charge. The charge transfer ratio, thus the ideal voltage conversion ratio, is determined by the SC converter topology. To generate a wide range of output voltages, converters with configurable topologies are used [44]. Various output voltage levels can be generated by controlling the amount of charge stored in the flying capacitor network with pulse width modulation, frequency modulation, or capacitance modulation.

A simple SC voltage converter that uses minimum number of switches and capacitors is the 1:1 converter, as shown in Fig. 2.4a. The complete operation of this SC converter is performed in two phases, phase 1 (PH1) and phase 2 (PH2). During PH1, the flying capacitor is charged to V_{in} and during PH2 this capacitor is discharged to the output load, providing 1:1 voltage conversion. Another topology, a 2:1 SC voltage converter that has four switches and a flying capacitor is shown in Fig. 2.4b. In this configuration, the flying capacitor is charged to $V_{in} - Vo$, forcing the output to settle at $V_{in}/2$. An ideal 2:1 SC converter can provide 100% efficiency when the output voltage is $V_{in}/2$ at no load condition. When a finite amount of current is provided to the output load, the output voltage reduces below the desired V_o, reducing the power efficiency of the converter. The power efficiency of an SC converter is therefore fundamentally limited to V_o/nV_{in} where n is the voltage conversion ratio. A detailed analysis of the fundamental power efficiency limitations of SC voltage converters is provided in [45, 46]. This topology related power efficiency limitation has motivated the researchers to design configurable SC converters that can support multiple topologies with a single design to provide high power efficiency over a wide input and output voltage range.

Other than the topology related fundamental power efficiency limitation, parasitic losses of SC converters reduce the power efficiency of the converter. These power loss mechanisms include: i) switch driving loss, ii) switch buffer loss, iii) parasitic losses, and iv) control and reference losses.

2.3.1.1 Switch Driving Loss

The switches within an SC converter are implemented with MOS transistors. A finite amount of power is dissipated when the switches turn on and off. The power dissipated during the switching

activity is,

$$P_{SW} = C_{sw} V_{DD}^2 f_{sw}, \tag{2.1}$$

where the C_{sw} is the total gate capacitance of the switches, V_{DD} is the supply voltage, and f_{sw} is the switching frequency of the converter. The power dissipated during the switching activity increases with frequency and switch size. Since SC converters with a smaller flying capacitor require smaller switches, the switch driving loss is lower for smaller SC converters.

2.3.1.2 Switch Buffer Loss

When the flying capacitor and switches are large, a series of tapered buffers are used to drive each individual switch. The switch buffer loss is the power consumed by these tapered buffers. Buffer loss becomes important when the switch sizes increase and therefore must be included in the efficiency analysis. The total power dissipated within the tapered buffers is [47],

$$P_{Buff} = \sum_{i=1}^{i=N} C_{Desired} F^{i-1} V_{DD}^2 f_{sw}, \tag{2.2}$$

where the N is the optimum number of stages, $C_{Desired}$ is the desired load of the VCO, and F is the optimum fanout of each stage. The power dissipated within the tapered buffers exhibits a similar behavior with the switching power loss and increases with the switching frequency and flying capacitor size.

2.3.1.3 Parasitic Capacitance Losses

A significant amount of power is wasted to charge and discharge the parasitic capacitance of the flying capacitor and switches. The main contributor of the power loss is the bottom plate capacitance of the flying capacitor. For example, in a 2:1 SC converter, the bottom plate of the flying capacitor is charged to V_o during charging phase and is discharged to ground during the charge transfer phase. In other words, a relatively large parasitic capacitor is charged and discharged at every cycle, significantly reducing the overall power conversion efficiency. Since the highest possible power is dissipated when the parasitic capacitance is charging and discharging between the output

voltage and ground, the related power loss is,

$$P_{Par} = C_{BottomPlate} V_o^2 f_{sw}, \tag{2.3}$$

where $C_{BottomPlate}$ is the total bottom plate capacitance and V_o is the output voltage of the converter. The power loss due to the parasitic capacitance scales with the size of flying capacitance and switching frequency.

2.3.1.4 Control and Reference Losses

Another loss mechanism is the power dissipated within the related control and reference circuits. Finite amount of power is consumed to: i) generate the reference voltage, ii) compare the output voltage with reference to provide feedback, and iii) generate the feedback signal. The control and reference circuit related power losses $P_{Control}$ can be considered constant over a wide current range with little or no dependence to output voltage or output current.

The overall power efficiency of a conventional SC voltage converter is,

$$\eta_{SC} = \frac{P_{out}}{P_{out} + P_{SW} + P_{Buff} + P_{Control} + P_{Par}}, \tag{2.4}$$

where P_{out} is the output power of the converter. (2.4) is used in the rest of the work to analytically determine the efficiency of the proposed system. A more comprehensive power efficiency analysis can be found in [48].

2.3.2 Power Efficiency of SC Converters with Different Flying Capacitor Values

A decision flow similar to [48] has been used to determine the optimum switching frequency that provides a certain output voltage of a 2:1 SC converter. First, the required output impedance to generate a certain output voltage under a given output current load is determined. The optimum switching frequency to obtain the required output impedance at a particular output current and power efficiency is then obtained using (2.4).

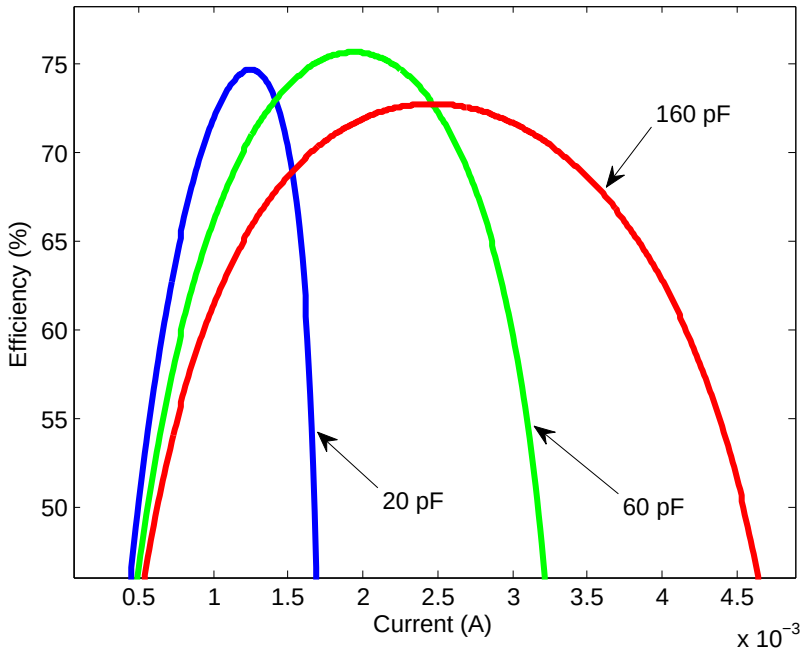


Figure 2.5: Power conversion efficiency of various SC voltage converter with different flying capacitor values. A smaller converter provides maximum power efficiency when the load current is lower whereas a larger converter can provide better efficiency under higher output current.

The power efficiency of differently sized 2:1 SC voltage converters with flying capacitors of 20 pF, 60 pF, and 160 pF when the load current ranges between 0.1 mA and 5 mA is illustrated in Fig. 2.5. Note that the switches and tapered buffers are scaled based on the size of the flying capacitor. A tapering factor of $\sim$2.5$\times$ is used in the analysis. A quite important result observed from Fig. 2.5 is that SC converters with different flying capacitor values provide the maximum possible power efficiency under different load currents. An SC converter with a smaller flying capacitor provides a high power efficiency when the load current is low because the tapered drivers and buffers used in the configuration are smaller. Alternatively, an SC converter with a larger flying capacitor can provide higher power efficiency under a larger load current. A flat power efficiency curve can therefore be achieved if the size of the SC converter is adaptively modified based on the workload.

2.3.3 Converter-Gating and Distribution

Interleaved SC converters typically utilize frequency modulation, capacitance modulation, or pulse width modulation to provide a constant output voltage under transient load currents [27, 44, 45]. However, these control techniques do not guarantee high power efficiency when the load current is low. At low load currents, the power efficiency is significantly degraded since the power dissipated in the control circuitry and parasitic impedances becomes significantly higher as compared to the load current.

Based on the observations that smaller SC converters are more efficient at lower load currents whereas larger SC converters are more power efficient at higher load currents, a new converter-gating technique is proposed in this paper. Since most of the SC converters are interleaved, each interleaved stage is turned on and off to provide a specific type of capacitance modulation as a coarse control technique. Frequency modulation is used as a fine control technique to regulate the output voltage between capacitance steps. This proposed approach increases the power conversion efficiency by forcing each stage to operate at the highest achievable power efficiency. The proposed voltage converter control technique therefore achieves a higher power efficiency as compared to the existing techniques which typically employ either capacitance or frequency modulation. To deactivate an individual converter stage, certain switches within an SC converter stage are turned off, isolating the input and connecting the flying capacitor to the output node. The implementation cost of the proposed converter is negligible as the components of the proposed converter-gating technique are already implemented in a conventional interleaved SC converter. The only additional circuit is a simple decoder that turns the stages on and off.

The interleaved stages of the converter are distributed throughout the power grid to act as local voltage converters. Distributing individual converter stages reduces the parasitic impedance between the converter and load circuits and therefore reduces the IR and Ldi/dt voltage drop. Additionally, the response time of the converter to transient load changes is improved due to the reduced power grid parasitic impedance between the converter and the load.

The primary overheads of the proposed converter-gating technique, assuming that the system already has on-chip voltage regulation, are summarized below.

2.3.3.1 On - Off Transition Time of Individual Regulators

As individual interleaved stages of the regulator turn on and off depending on the output current, the activation and deactivation time of these stages must be sufficiently short to not disrupt the operation of the circuit. A control technique is proposed in Section 2.4 that permits a 2:1 SC converter to behave as a 1:1 SC converter for a short time to reduce the activation time of an individual stage. This technique improves the charge transfer ratio for a couple of cycles to transfer the required charge to the output node faster.

2.3.3.2 Area Overhead

Assuming that the circuit already has control circuitry for power/clock gating, and on-chip sensors and performance counters, the area overhead of the converter-gating will be the additional control circuitry and one decoder to control the activity of the individual converter stages.

2.3.3.3 Power Overhead

The modified control circuitry and decoders slightly increase the power consumption which is significantly lower than the power savings with the proposed technique.

2.3.3.4 Output Noise

The output voltage ripple is increased due to the asymmetrical behavior caused by changing number of interleaved stages, which is given in Fig. 2.13. To minimize the output noise, the inactive stages are utilized as decoupling capacitors by connecting the flying capacitor to the output node, as explained in Section 2.5-C.

The primary strength of the proposed technique is that the power conversion efficiency is increased over 5% with slight modifications to the existing on-chip voltage regulation system.

2.4 Circuit Level Design of Converter-Gating

The proposed method is designed using IBM 130 nm technology kit. The proposed converter-gating methodology is explained in Section 2.4.1. The impact of distributing individual interleaved

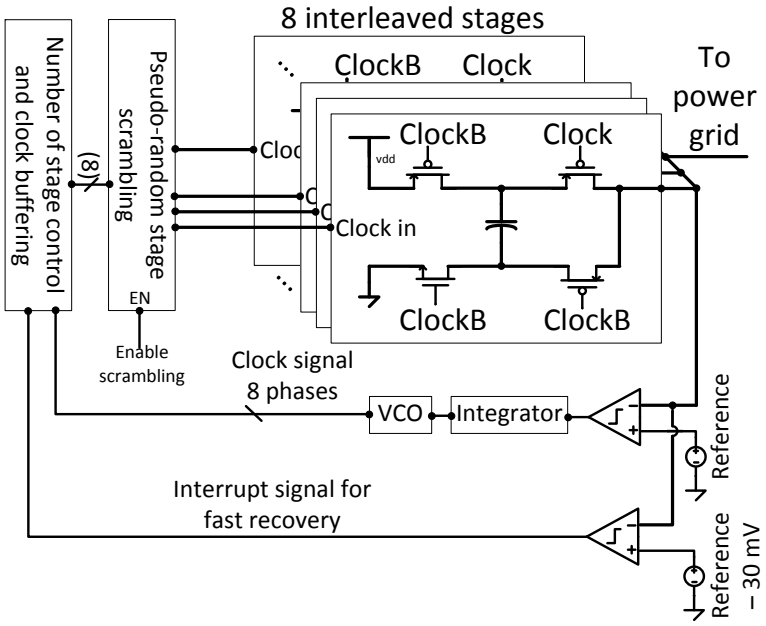


Figure 2.6: Top level schematic of the proposed converter-gating system.

stages on the power noise is discussed in Section 2.4.2. The proposed configurable 2:1 to 1:1 SC converter is presented in Section 2.4.3. The exploitation of the proposed converter-gating technique as a countermeasure against side channel power attacks is explained in Section 2.4.4.

2.4.1 Converter-Gating Control Methodology

The complete converter-gating control structure is shown in Fig 2.6. MOS capacitors are used as flying capacitors within the 2:1 SC converter. The converter uses two comparators to create feedback signals for the control loop. One comparator compares the output voltage with the reference voltage and the comparator output is integrated to create the control voltage for the voltage controlled oscillator (VCO), which is realized as a current limited inverter chain. The second comparator detects transient load changes that would result in more than 30 mV voltage drop. In this case an interrupt is triggered and its operation is explained in Section 2.4.3. The control logic determines the optimum number of active stages and provides the required control signals to the interleaved SC voltage converter through a pseudo-random scrambling circuit. The scrambling circuit uses a pseudo-random number generator and scrambles the activation pattern of

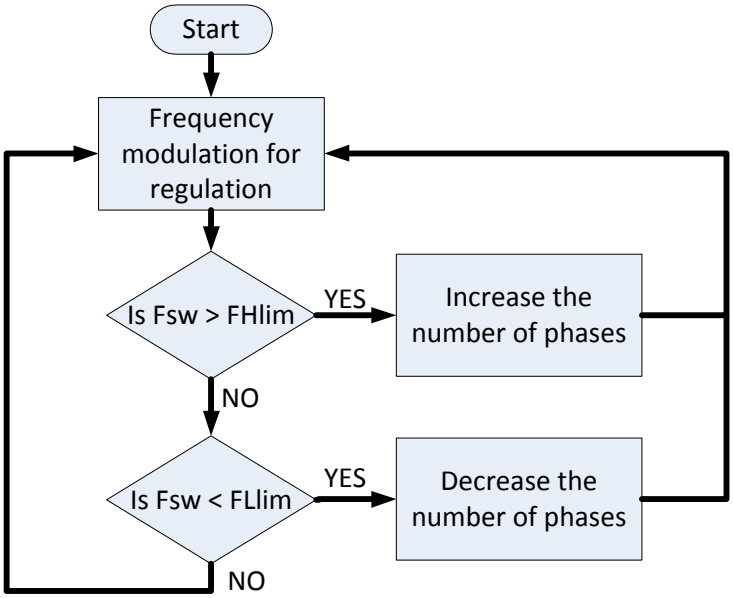
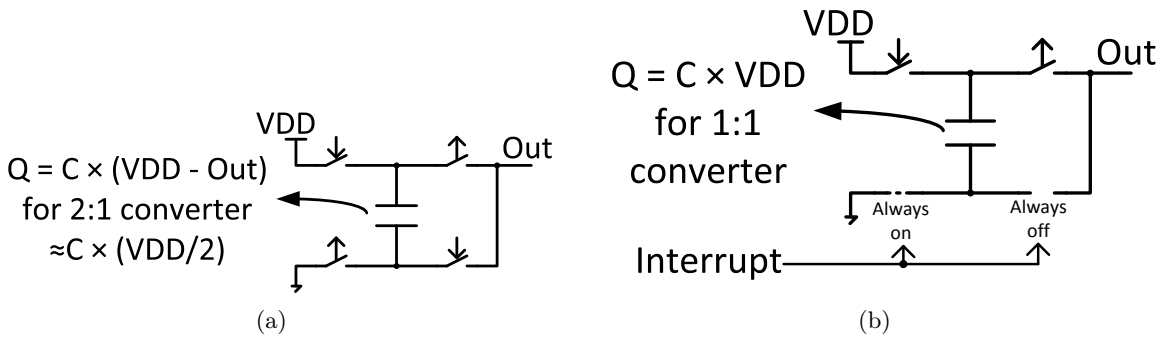


Figure 2.7: Proposed converter-gating algorithm that enables workload aware activity management of distributed SC voltage converters.

the individual stages. When certain converter stages are deactivated, each remaining active stage is effectively forced to operate at its maximum efficiency. Deactivated stages are connected to the output node and act as a decoupling capacitor to reduce the output voltage ripple. The algorithm used to determine the number of active converters is given in Fig. 2.7. When the switching frequency or the input voltage of the VCO exceeds a predetermined limit $FHlim$ (60 MHz) for more than 5 cycles, an additional converter stage is activated. Alternatively, when the switching frequency becomes lower than a certain limit $FLlim$ (30 MHz) for more than 5 cycles, a converter stage is deactivated. To prevent stages from turning on and off randomly when the control signal is at limit values, a hysteresis loop with 10 MHz width is implemented. The frequency limits are selected as 60 MHz and 30 MHz to optimize the power density and efficiency according to [48]. In the proposed control, the activity of individual converter stages is utilized as a coarse control technique whereas the switching frequency is used as a fine control technique. For example, if the load current demand increases when certain number of stages are active, the operating frequency increases to provide the required load current. If the frequency exceeds the upper frequency limit $FHlim$ (60 MHz), another individual stage turns on, which in turn reduces the switching frequency. The 30 MHz and 60 MHz



(a) (b)

Figure 2.8: Amount of charge transferred to the output note in a single cycle for a) a conventional 2:1 SC voltage converter and b) a 2:1 converter that is configured as a 1:1 converter by controlling the illustrated switches. 1:1 configuration provides two times more charge to the output node in a given cycle, improving the response time.

limits imply that each converter stage delivers an output current between ∼80 uA and ∼350 uA. When converter stages are forced to deliver more than ∼350 uA or less than ∼80 uA, frequency exceeds 60 MHz or goes below 30 MHz, turning on or off another stage and keeping the frequency in 30 MHz - 60 MHz range.

2.4.2 Distribution of the Interleaved Stages

Each interleaved stage of the SC converter is uniformly distributed throughout the power grid to minimize the power noise and enable point-of-load voltage regulation. The physical location of the active SC stages is important to reduce the power noise. Based on the information provided by local voltage and current sensors, performance counters and temperature sensors, a specific voltage regulator can be turned on or off using the proposed algorithm. The implication of distributing individual interleaved stages on the power noise is analyzed with extensive simulations in Section 2.5.3.

2.4.3 Configurable SC Voltage Converter

A new control technique is proposed to adaptively configure the conversion ratio of an SC voltage converter for a couple of clock cycles to speed up the activation and deactivation of individual stages. To achieve a fast recovery during either activation (deactivation) of individual

stages or transient voltage drop (bounce), it is necessary to transfer a higher (lower) amount of charge to the output node for a finite amount of time. Introducing interrupts and fast loops has been used in [27, 49]. However, a convenient and simple technique to achieve fast response time is configuring a 2:1 converter as a 1:1 converter during the load transients. During the normal operation of a 2:1 converter, the flying capacitor is charged to as high as $V_{in} - V_o$. Alternatively, if a 1:1 configuration is used, the total charge can be increased by $C_{flying} \times V_o$. By configuring a 2:1 converter as a 1:1 converter, the total amount of charge transferred to the output node in each cycle is increased nearly by a factor of two, significantly reducing the response time. One of the advantages of this configuration technique is that most of the existing voltage converters can be adaptively configured as a 1:1 SC converter, reducing the implementation cost of the proposed approach to only a decoder in digital domain and a comparator to generate interrupt signals. The working principle of the proposed method is explained in Fig. 2.8. During the transients, when the interrupt signal is given, the switch connected to ground remains on, and the switch connected between the bottom plate of the flying capacitance and the output remains off, effectively configuring the 2:1 converter as a 1:1 converter, increasing the amount of charge transfer to the output node per unit time. Using this approach may generate output voltages higher than the desired voltage, which in turn may cause instability. Therefore the drop voltage (30 mV) must be selected carefully to prevent the 1:1 converter from generating higher voltages than the desired output voltage even under worst case conditions.

2.4.4 Converter-Gating as a Side-Channel Attack Countermeasure

The relationship between the input current and load current profiles is linear for LDO regulators, as shown in Fig 2.15b. Alternatively, switching converters have an input current that consists of current spikes whose amplitude, frequency, and width depends on the control signal generated by the feedback loop. Due to this complicated relationship between input and output current profiles of an on-chip switching converter, a decipher requires more time and effort to understand the functionality or the stored secret key. The relation between the input and output currents becomes even more complicated when the proposed converter-gating approach is used. The

frequency and amplitude are no longer linearly correlated with the load current since the frequency and amplitude of the spikes adaptively vary during the operation as the number of active stages change. Although the input current and power waveforms are more sophisticated to analyze even with a conventional SC voltage converter, the overall power consumption can be further convoluted by randomizing the activation pattern of the individual stages.

A *randomized* converter-gating technique is proposed in this section to minimize the correlation between the input and load current profiles. The activation pattern of the individual stages within the proposed SC converter system is determined with a linear feedback shift register (LFSR) based 10-bit pseudo random number generator. As a result, a random delay is inserted to the input current waveform and the amplitude of the spikes randomly varies with the activation pattern. For example, when five interleaved stages are active, the phases of these active stages can be configured as (0°, 45°, 90°, 135° and 180°) or (0°, 90°, 180°, 225°, and 270°) ($\binom{8}{5}$=56 different combinations exist for this case). These different converter-gating activation patterns lead to varying current spikes at the input current of the SC voltage regulator. In the proposed SC voltage converter, the operating frequency is 30 MHz while delivering 1.5 mA. Therefore, by using a randomized converter-gating pattern, the effect of the load transient on the input current at each clock edge is pseudo-randomly delayed between ∼4.125 ns and ∼20 ns.

2.5 Functional Verification of Converter-Gating

An eight stage 2:1 SC voltage converter is designed with 130 nm IBM CMOS technology. The top level schematic of the complete design is illustrated in Fig. 2.6. Each individual converter stage has a 20 pF flying capacitor (implemented using MOS capacitors) to allow a total output current between 200 uA and 2.5 mA. Although a conventional 2:1 SC voltage converter is used, the controller of the switches is designed to permit this 2:1 converter configurable as a 1:1 converter, as shown in Fig. 2.8.

The overall power efficiency of the proposed power delivery system is evaluated in Section 2.5.1. The response time of the proposed configurable 2:1 to 1:1 SC converter is evaluated in Section 2.5.2. The effect of distributing voltage regulators on the power supply noise is investigated

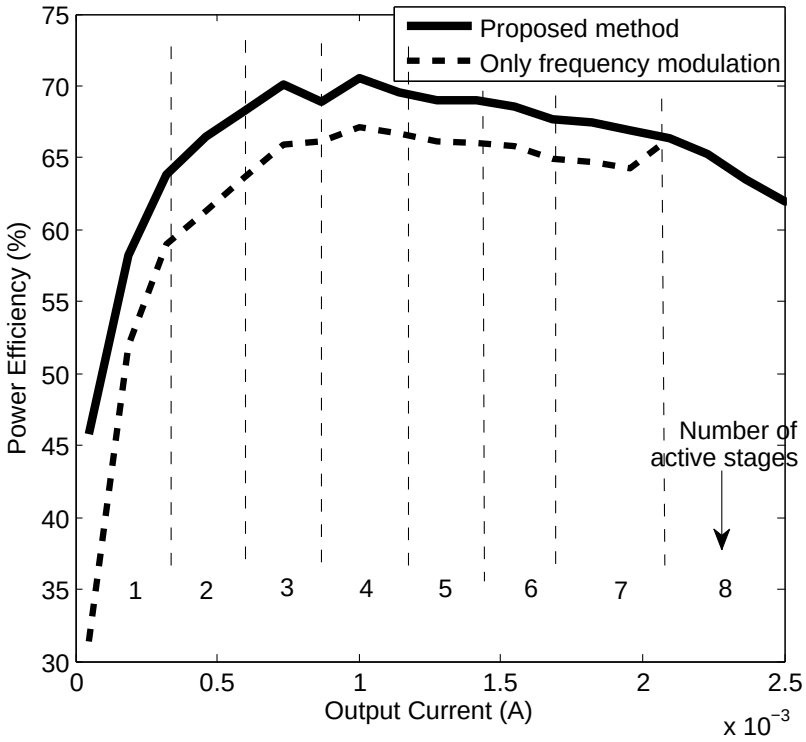


Figure 2.9: Power conversion efficiency of an eight stage interleaved SC voltage converter with and without applying the proposed converter-gating technique. The power conversion efficiency is increased ∼5% with negligible area overhead by utilizing the proposed technique.

in Section 2.5.3. The implications of gating certain interleaved stages on the voltage ripple are analyzed in Section 2.5.4. The proposed converter-gating is exploited as a secure on-chip power delivery architecture in Section 2.5.5.

2.5.1 Power Efficiency

The power efficiency of the proposed SC converter system utilizing the proposed control technique is evaluated when the load current is swept between 200 uA and 2.5 mA while providing 550 mV from a 1.2 V supply. The efficiency of the power delivery network is given in Fig. 2.9 where the solid and dashes lines, respectively, show the power efficiency of the voltage converter utilizing the proposed method and the power efficiency of the converter when all of the eight stages are always active and only frequency modulation is used. The results indicate more than 5% savings in power conversion efficiency by utilizing the proposed converter-gating technique.

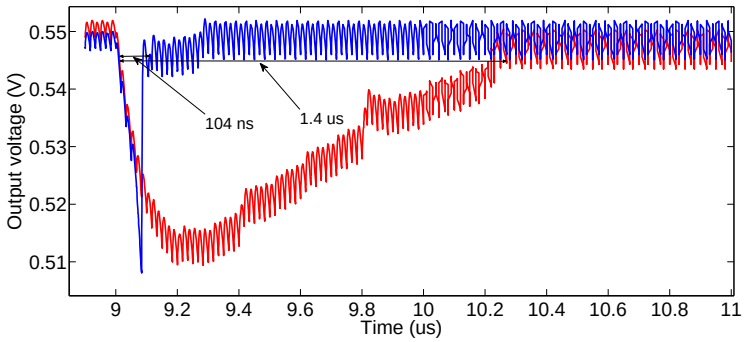


Figure 2.10: Transient response of a 2:1 SC converter when the load current increases from 1 mA to 3 mA. The response time for a conventional 2:1 SC voltage converter (shown in red) is 1.4 μs. When the proposed adaptively configurable voltage converter, shown in Fig. 2.8 is used, the response time reduces to 104 ns.

2.5.2 Configurable 2:1 to 1:1 SC Voltage Converter

The proposed configurable 2:1 SC converter, illustrated in Fig. 2.8, is evaluated when the load current increases from 1 mA to 3 mA. When the output voltage falls 30 mV below the desired output voltage, the interrupt signal is asserted to configure the 2:1 converter as a 1:1 converter. The system is configured as a 1:1 converter in less than 30 ns, which improves the response time of the converter from 1.4 us to 104 ns, as shown in Fig. 2.10.

2.5.3 Voltage Maps of the Power Grid

The impact of distributing individual stages of the interleaved SC voltage converter is evaluated with a 23×23 uniform power grid and without using the scrambling method. Eight individual converter stages and multiple load current sources are uniformly distributed throughout the power grid. The voltage map of the power grid when all of the phases of an eight stage SC converter are connected to the center of the power grid is shown in Fig. 2.11a. When each individual phase of an eight stage SC converter is uniformly distributed throughout the power grid, the voltage map is given in Fig. 2.11b. In both cases, the voltage converters provide a total of 2.5 mA output current to the load circuits. The centralized converter has a maximum voltage drop of $\sim$50 mV at the nodes far away from the center of the power grid. The maximum voltage drop reduces to $\sim$15 mV when the individual stages are distributed while also reducing the voltage gradient.

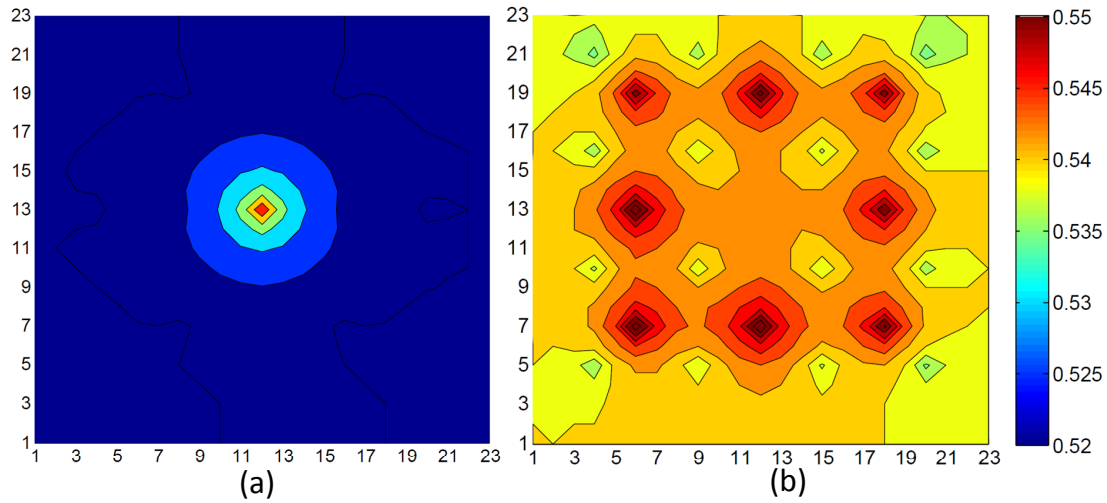


Figure 2.11: Voltage map of the power grid when the load circuits are uniformly distributed. a) All of the eight stages of an SC voltage converter are connected to the center of the power grid. b) All of the eight stages of an SC converter are distributed uniformly.

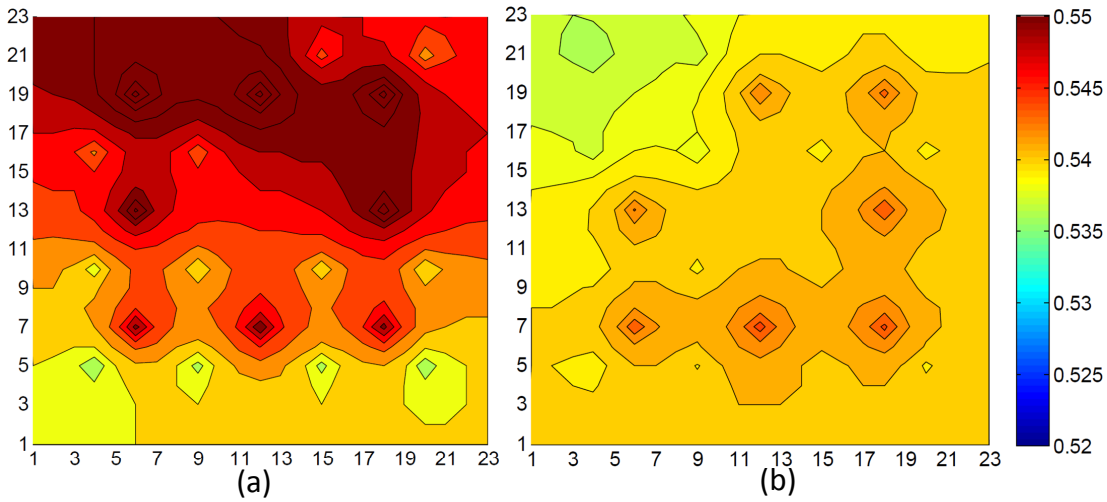


Figure 2.12: Voltage map of the power grid when the load circuits located at the upper-left corner of the power grid enters idle state and all of the eight stages of an SC converter are distributed uniformly. a) All of the converter stages are active . b) Individual voltage converter stages that are close to the idle circuit block are deactivated with the proposed converter-gating technique.

When a circuit block enters idle mode of operation and the total load current reduces such that the proposed algorithm forces an SC converter stage to turn off, the nearest converter stage to the idle circuit block is deactivated. The voltage map for the same power grid is determined for two additional cases when a circuit block located at the upper-left corner of the power grid

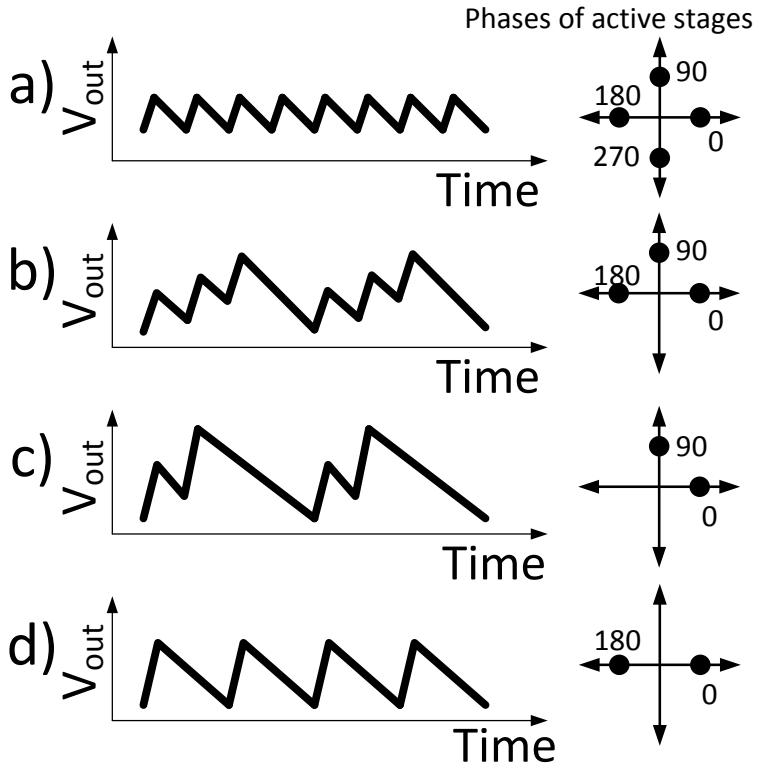


Figure 2.13: Output voltage ripple of a four phase interleaved SC voltage converter with different number of active stages. a) All stages are active. b) One stage is deactivated. c) Two adjacent phases are deactivated. d) Two symmetric phases are deactivated.

enters idle mode of operation. In the first case, as shown in Fig. 2.12a, all of the the converter stages remain active but the frequency is reduced to provide a lower load current. In the second case, as shown in Fig. 2.12b, the converter stage that is closest to the idle circuit is turned off with the proposed algorithm to reduce power conversion loss. These results illustrate that even though using only frequency control provides a slightly lower maximum voltage drop of 6 mV as compared to the proposed technique, converter-gating secures more than 5% power savings during voltage conversion.

2.5.4 Output Voltage Ripple

Interleaved voltage regulation has been widely used for output voltage ripple reduction. When certain interleaved stages are deactivated, the output voltage ripple exhibits an asymmetric

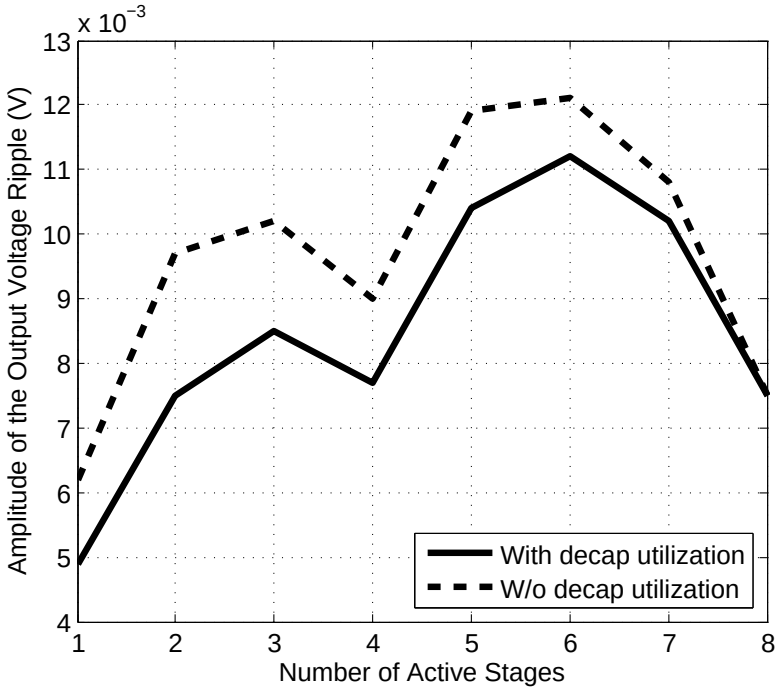


Figure 2.14: Amplitude of the output voltage when the inactive converter stages are utilized as decoupling capacitor (solid line) and without decoupling capacitor utilization (dashed line). 20% reduction in the output voltage ripple can be achieved with the proposed decoupling capacitor utilization.

behavior, as illustrated in Fig. 2.13 for a four stage interleaved SC converter. When all of the stages are active, the voltage ripple exhibits a symmetric behavior, as shown in Fig. 2.13a. When one of the stages is turned off, the output ripple becomes asymmetric and the amplitude of the ripple increases, as shown in Fig. 2.13b. When two of the four stages are turned off, there are two cases: If the deactivated two phases are adjacent to each other (*i.e.*, the phase difference is 90°), the output voltage ripple exhibits an asymmetric behavior, as shown in Fig. 2.13c. In the other case, when the deactivated two phases are symmetric to each other (*i.e.*, the phase difference is 180°), the output voltage ripple exhibits a symmetric behavior, as shown in Fig. 2.13d.

In the proposed technique, the output voltage ripple is reduced by utilizing the flying capacitors within the deactivated stages as decoupling capacitors. Utilizing these unused capacitances of deactivated stages can provide up to 20% reduction in the output voltage ripple amplitude without consuming any power. The output voltage ripple of an eight stage interleaved SC voltage converter

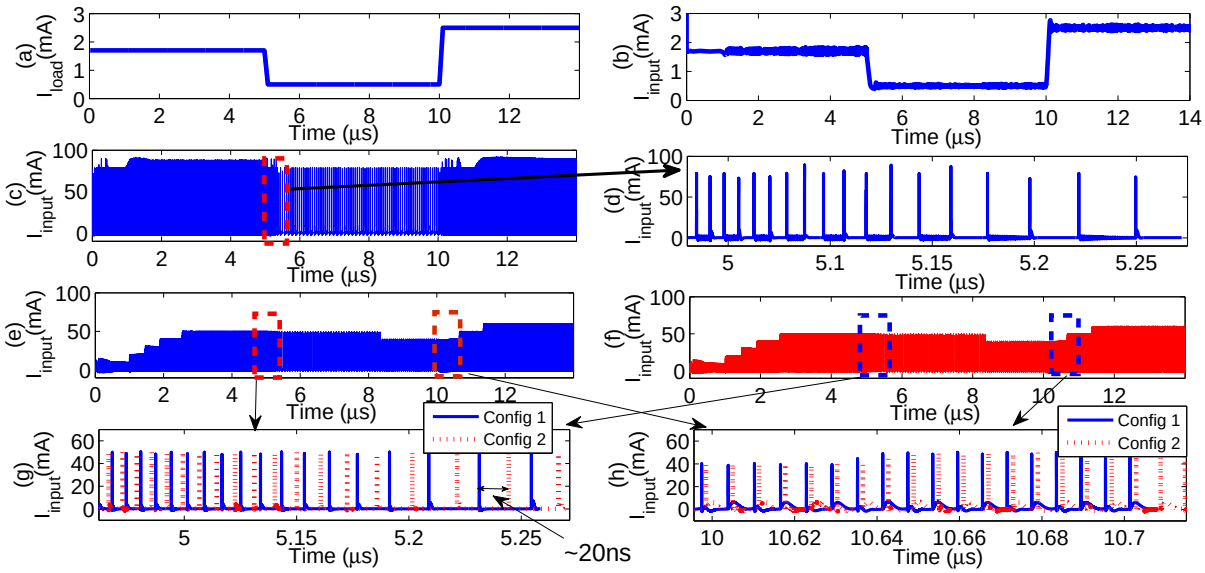


Figure 2.15: Load current profile and corresponding input current profile for various voltage regulation schemes. a) Load current profile. b) Input current profile when an LDO regulator is used. c) Input current profile when an eight phase conventional SC converter is used and d) a zoomed version of the current profile during transients. Input current profile when the proposed turn on and off patterns of the converter-gating technique is configured with e) Config 1 and f) Config 2. Zoomed version of the input current profile during g) fall transition and h) rise transition of the load current.

has been evaluated when the number of active stages varies between one and eight, as shown in Fig. 2.14 where solid line shows the output voltage ripple of the proposed method with capacitance utilization and dashed line shows the output voltage ripple of the proposed method when the flying capacitances of the inactive stages are left floating. The amplitude of the voltage ripple reaches a local minimum when four stages are active because at this point the remaining four active stages form a symmetric ripple behavior. Additionally, the amplitude of the voltage ripple reduces: i) when only one stage is active due to the quite low load current and ii) when all the stages are active due to the symmetricity of the phases.

2.5.5 Input Current Scrambling with Pseudo-Random Converter-Gating

To validate the proposed converter-gating technique as a countermeasure for side-channel attacks, the overall power consumption of a sample circuit is analyzed when the load current varies between 0.5 mA to 2.5 mA, as shown in Fig. 2.15a. An important observation obtained from this

analysis is that the power dissipation profile of an integrated circuit varies significantly depending on the type of the on-chip voltage regulator. To highlight the impact of the type of the voltage regulator on the power profile under the same current load, three different on-chip voltage regulation schemes are evaluated. First, a fully on-chip LDO voltage regulator is used to provide the required load current. The input current of the LDO regulator linearly changes with the load current and therefore exhibits a high correlation with the load current waveform, as shown in Fig. 2.15b. If a conventional LDO regulator is used without employing any countermeasure, the attacker can easily determine the power consumption profile of an IC.

In the second case, a conventional eight phase SC voltage converter is used to provide the required load current. Although the correlation between the input and output current waveforms is weaker with an SC voltage regulator, as shown in Fig. 2.15c, the frequency and amplitude of the input current waveform of an SC converter are still functions of the load current. For example, when the load current reduces from 1.7 mA to 0.5 mA at 5 us, the amplitude and frequency of the input current spikes reduce, as seen in Fig. 2.15d, which provides a zoomed version of the transient input current waveforms around 5 us.

In the proposed converter-gating based countermeasure, the time domain response is scrambled by pseudo-randomly selecting the turn on and off pattern of the individual converter stages. Without loss of generality, the input current waveforms are illustrated in Figs. 2.15e and 2.15f when the individual stages of the SC converter are activated based on two sample random activation patterns. These two sample configuration patterns (*i.e.*, Config 1 and Config 2) follow, respectively, the sequence 0°, 45°, 90°, 135°, 180°, 225°, 270°, 325° and 0°, 135°, 270°, 225°, 90°, 325°, 45°, 180°. Although the input current profiles of these two configurations, shown in Figs. 2.15e and 2.15f, seem similar, a random time delay is inserted between the input current spikes. $\sim$ 20 ns delay uncertainty is successfully inserted between the input current spikes by randomizing the converter-gating pattern, as shown in Figs. 2.15g and 2.15h. By randomly switching between various converter-gating patterns, the effects of load transients on input current from power supply can be reduced dramatically.

2.6 Conclusions

A secure and efficient power management technique, converter-gating, is proposed in this paper. Converter-gating increases efficiency and power analysis based side attack security by adaptively controlling the activity of individual stages within an interleaved on-chip SC voltage converter. Converter-gating technique increases the power conversion efficiency ∼5% and reduces the voltage drop more than 3× when distributed approach is used. By utilizing the proposed adaptive configuration technique, the response time of a 2:1 SC voltage converter to transient load changes reduces from 1.4 μs to 104 ns. The turn on and off pattern of the individual interleaved stages are randomized to scramble the power consumption profile as a countermeasure to side-channel attacks without consuming additional power. The timing of the input current profile is scrambled by adding ∼20 ns timing uncertainty.

CHAPTER 3:
TRANSIENT RESPONSE ANALYSIS OF RECONFIGURABLE AND RESPONSE ENHANCED CONVERTERS AND TECHNIQUES TO IMPROVE RESPONSE TIME

3.1 Introduction

The advancements in integrated circuit (IC) processing has provided circuit designers with tools to implement the most of the analog and digital circuits together on a single IC. Integrating most of the functionality on a single device and creating a system on chip (SoC) provides significant advantages over the discrete alternative as the reliability is improved and the size of the final system is reduced. However, full integration also introduces new challenges in power management due to the diverse requirements for the optimum supply voltage level and noise tolerance. To achieve the best power/performance tradeoff for every sub-system on a fully integrated SoC, dedicated power management solutions is required for each sub-system. The primary challenges for on-chip power management is to optimize the power efficiency while delivering a high-quality supply voltage. Dynamic voltage scaling (DVS) is widely used to adaptively allocate the available power budget to different cores to optimize the power efficiency and performance tradeoff [50–53]. To minimize power/ground noise and to maximize the power savings in DVS the power delivery network has to respond to load transients quickly while maintaining the desired output voltage level. Implementing dedicated power management circuitry at the printed circuit board (PCB) which can perform fast DVS for different circuit blocks and fast transient recovery may not be feasible since doing so requires a large number of dedicated pins and PCB area. Even if a PCB level solution is chosen, implementation of such systems may be limited in terms of speed since the package and PCB parasitic impedance limits the maximum achievable performance. A solution to this problem is

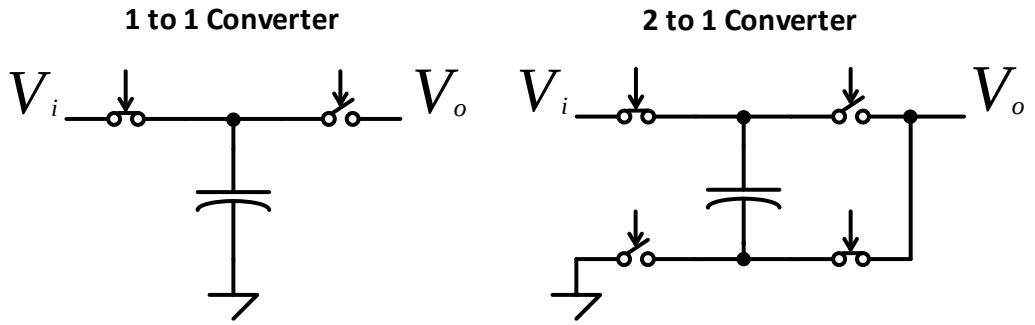


Figure 3.1: Comparison of 1/1 and 1/2 SC converters with abstract switches. Different topologies inherently settle at different output voltages at which they provide maximum efficiency.

fully integrating the voltage regulators (*i.e.*, DC-DC conversion and regulation for each sub-system) into the chip [54, 55].

There are several alternatives for implementing an on-chip DC-DC converter with regulation capabilities, such as low dropout regulators (LDO), inductor based switching converters, or switched capacitor (SC) converters [9, 56]. LDOs have high power density, fast response to transients, and can be implemented in any IC process using a standard library. However, LDOs suffer from limited power efficiency when DVS with a wide voltage range is required as the maximum power efficiency is limited to the voltage conversion ratio V_{out}/V_{in}. Alternatively, inductor based switching converters offer high power density and high power efficiency over a wide range of input and output voltages. However, the on-chip implementation of inductors is quite challenging in standard processes, reducing both the performance and scalability of inductor based voltage converters. The SC converters offer a scalable solution for diverse power requirements and provide medium-to-high power density and high efficiency [9, 56]. While the SC converters benefit from processes that have dedicated high density capacitors [57], they can also be implemented in standard processes without requiring any additional process. Due to these advantages over other topologies, SC converters have recently gained attention [58–61] and will therefore be the focus of this work.

One important characteristic of SC converters is that the voltage conversion ratio is determined by the topology. A 1/1 converter, as shown in Fig. 3.1a, has a capacitor that is charged to

the input voltage in phase 1 and discharged to the output in phase 2, directly replicating the input voltage at the output node in steady state when no load is connected. A 1/2 converter, however, has a capacitor that is charged to the difference of the input and output voltages in phase 1, and discharged to the output in phase 2. In the steady state, assuming no load is present at the output, the output voltage settles at half of the input voltage according to Kirchoff's voltage law (KVL). Different conversion ratios can be implemented using different topologies as covered in [62, 63]. If a single conversion ratio is used, the power conversion efficiency would be lower when the output voltage is lower than the ideal output voltage since the capacitors will be charging and discharging between a larger voltage difference and the charging of a capacitor through a switch is not 100% efficient [64]. To achieve high conversion efficiency over a wide range of input and output voltages, reconfigurable SC converters are used [55, 58, 65]. Reconfigurable converters achieve different voltage conversion ratios by using the same capacitors and modifying the switching pattern of the switches. The converter can therefore be configured to operate at the desired voltage conversion ratio depending on the available input and required output voltage levels.

Since reconfigurable converters offer flexibility on the input and output voltage range, these converters can be quite advantageous in DVS systems while optimizing the operating conditions of diverse sub-systems in an SoC [65]. Furthermore fully integrated reconfigurable converters can provide fast transient recovery that lowers the power supply noise and fast response to the changes in the reference voltage. These converters can scale the supply voltage level swiftly, facilitating fast DVS operations which in turn offer higher system level power savings [50–52]. However, the response characteristics of these converters have previously been investigated using a single configuration and the implications of the reconfiguration on the stability and response time of these converters have not been addressed in the literature. The primary objective of this chapter is to provide an analysis of the reconfiguration on the response time, especially around the boundaries of operating regions of different conversion ratios. The conditions that occur at the boundaries of different conversion ratios bear resemblance to several response time enhancement techniques proposed in literature [49, 57, 66] which have similar issues during transient recovery and therefore are analyzed in this chapter.

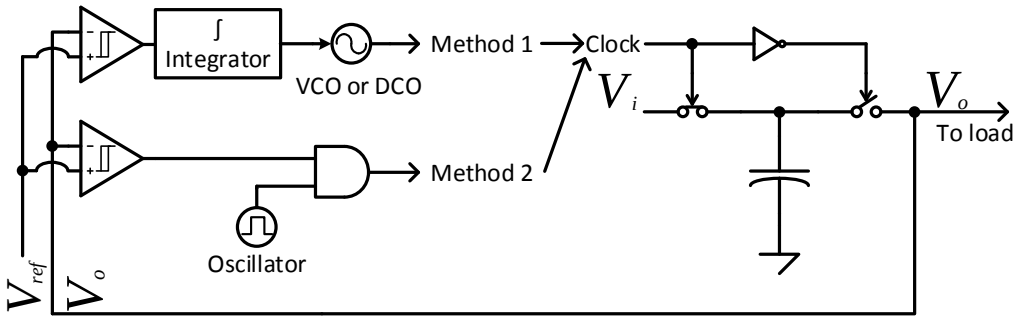


Figure 3.2: Conventional methods to implement control loops for SC DC-DC converters. Method 1 uses a voltage controlled oscillator or a digitally controlled oscillator to generate the control frequency and Method 2 uses clock gating to generate the control frequency. Method 1 is desired for low output voltage ripple whereas Method 2 is used when a simple solution is needed.

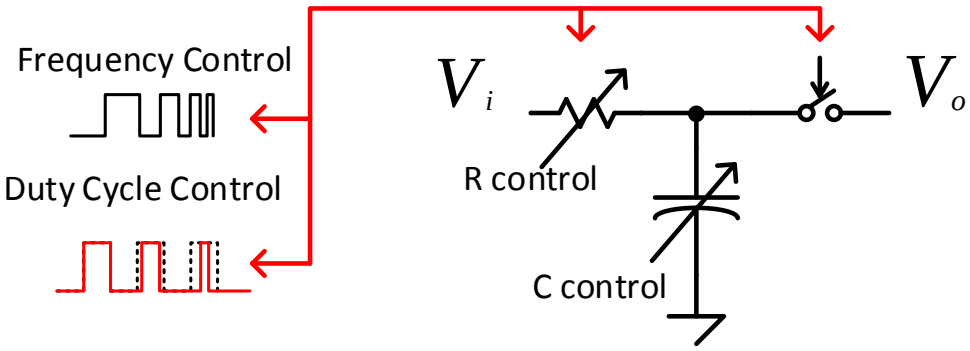


Figure 3.3: Some of the converter parameters that are used in regulation.

The rest of the chapter is organized as follows. In Section II, charge transfer rate of a 1/1 SC converter configuration is analyzed and this analysis is extended to cover other conversion ratios. In Section III, the transient response of reconfigurable converters during transients that require reconfiguration and the transient response of converters with transient response enhancements are examined. In Section IV, a new control technique is proposed to address the transient response issues and conclusions are offered in Section V.

3.2 Analysis of Dynamic Behavior in SC Voltage Converters

To understand how an SC voltage converter operates, an analysis of SC converters under varying operating conditions such as different conversion ratio and different frequency is performed. Although there are several studies in literature that cover the analysis of SC voltage converters [63, 64, 67–69], the focus has typically been on optimizing the efficiency and determining the optimum conversion ratios, rather than using the analysis to investigate the transient response of the converters. An analysis that extends the previous work to better explain the intricacies of operating conditions and transient response characteristics is developed. To the best of the authors' knowledge, this is the first study on the transient behavior of a reconfigurable SC converter considering the effects of the boundary conditions between different conversion ratios. In this section, first, the regulated SC converter will be introduced. Then the charge transfer rates based on the parameters used in regulation (*i.e.* frequency) is determined for several conversion ratios. Finally, the implications of the difference in charge transfer rates at the boundaries between different conversion ratios is discussed.

An SC converter with regulation capability consists of a control loop stabilizing the output voltage of the converter by modulating one of the following parameters; i) switch size (resistor), ii) capacitor size, iii) frequency of operation, and iv) duty cycle [70], as illustrated in Fig 3.3. By changing these parameters based on the workload, an SC converter can modify the amount of charge delivered to the output, effectively modifying the equivalent output impedance of the converter. To track the voltage level at the output and close the loop, a comparator and an integrator can be used, as illustrated as *Method 1* in Fig. 3.2. Alternatively, an on/off type controller, which usually includes only a comparator and an accompanying logic, can be utilized, as illustrated as *Method 2* in Fig. 3.2. A comparator-integrator loop is typically preferred over an on/off type controller for on-chip SC voltage converters since the comparator-integrator based control can considerably reduce the output voltage ripple [70]. A comparator-integrator based control mechanism will therefore be the used in this work.

Reconfigurable converters typically use the same control loop regardless of the conversion ratio as a comparator-integrator loop is capable of operating with different conversion ratios [8, 49,

55]. When the same loop is used for different conversion ratios, however, the loop has to adapt to the new charge transfer ratio of a different configuration during each transient. If the control loop is not modified based on the transient characteristics of different conversion ratios, the transient response may take significantly longer until the integrator starts following the charge transfer rate of the new conversion ratio. This may even cause instability if the conversion ratio is also being determined in another separate loop. Hence, the charge transfer characteristics of a reconfigurable converter at the boundary conditions between conversion ratios need to be investigated.

The charge transferred to the output per cycle and charge transferred to the output per second (output current) are chosen as the two metrics to characterize SC converters for transient response analysis because these metrics can be easily written as a function of the output voltage, frequency, flying capacitor value, and output decoupling capacitor value. The primary reason for not using the output resistance even though it is straightforward to calculate from the output current is because charge transfer rate is more intuitive to interpret at different configurations and output voltages.The accumulated output current on the decoupling capacitor determines the output voltage and therefore the transient behavior is easier to analyze mathematically using the output current rather than output resistance.

3.2.1 Analysis of the Ideal Voltage Conversion Ratio

3.2.1.1 Direct Analysis

To develop an understanding on how an SC converter works, first an intuitive analysis on a simple converter will be performed to obtain the ideal conversion ratio. For this purpose the 1/2 converter is chosen and this topology is given on Fig 3.9. The capacitor C_1 is called the flying capacitor which transfers charge to the output, also a second capacitor C_2 is added as decoupling capacitor with the voltage across it defined as output voltage. V_g DC supply acts as the input voltage to the converter. In the converter, the S_1 and S_3 (odd numbered switches) operate during one half of the clock while S_2 and S_4 (even numbered switches) operate during the remainder of the clock cycle. These two switching states will be referred as phase 1 (charging phase) and phase 2 (discharging phase) respectively. During phase 1 the flying capacitor C_1 is connected between the

input supply and the output as shown in Fig 3.9. According to Kirchoff's voltage law, equation 3.1 applies.

$$V_g = V_{C1} + V_{C2} \tag{3.1}$$

During phase 2 the flying capacitor C_1 is connected between ground and the output with the same polarity as shown in Fig 3.9. The equation 3.2 can be written for this phase.

$$V_{C1} = V_{C2} \tag{3.2}$$

Assuming the load current is negligible and that the converter is at its steady state, the two equations 3.1 and 3.2 can be combined, resulting in equation 3.3.

$$\begin{aligned} V_g &= 2V_{C2} \\ V_{C2} = V_{OUT} &= \frac{V_g}{2} \end{aligned} \tag{3.3}$$

This shows that the output voltage in steady state will be equal to the half of the input voltage. In more detail, the flying capacitor is being charged to the voltage difference between input and the output voltages and then discharged to the output voltage so the starting voltage in the charging phase is the output voltage to begin with, meaning that two times the output voltage is equal to the input voltage.

One important realization is that this analysis only works when there is no current is being sunk from the output which means that R_L is large. In a realistic application this is not usually the case and a certain amount of current is delivered to the load. As the current demand increases (R_L decreases) the voltage of C_2 at the end of the phase 2 will get lower, which means that the flying capacitor is charged to a higher voltage instead of half of the input voltage. This situation changes two important parameters in the previous analysis, firstly the output voltage now moves up and down as the input is disconnected during phase 2 and no extra charge other than the charge delivered by the flying capacitor is transferred. Charge delivery to the decoupling capacitor generates a sawtooth-like waveform at the output and is an important performance parameter. Secondly, the

voltage on the flying capacitor is no longer constant. Assuming that a complete charge transfer occurs at the end of the phase 2, the flying capacitor voltage is lower than half of the input voltage at the end of the phase 2. When the flying capacitor is connected between the input voltage and the output in phase 1, the voltage difference across its terminals are no longer half of the input voltage but a higher value. Naturally this implies that the flying capacitor is charged, discharged and delivered charge to the decoupling capacitor. However, this also implies that the flying capacitor is charged and discharged through switches, which means that the efficiency of this operation is now lower because of inherent losses in charging a capacitor through a switch. The ripple voltage and the reduction in efficiency will be further investigated.

3.2.1.2 Systematic Analysis

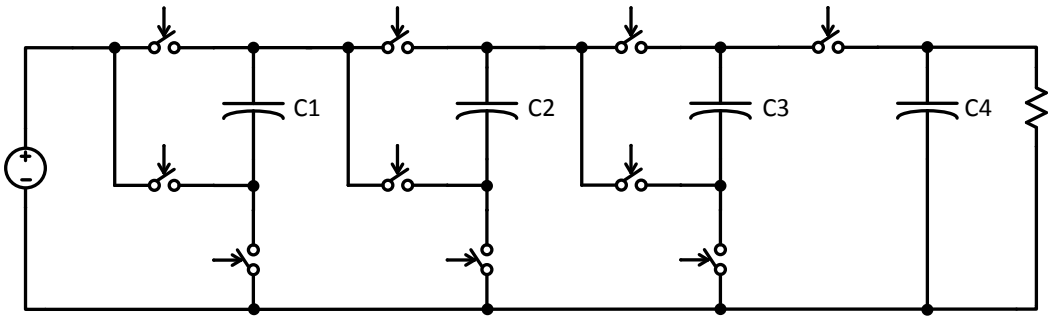
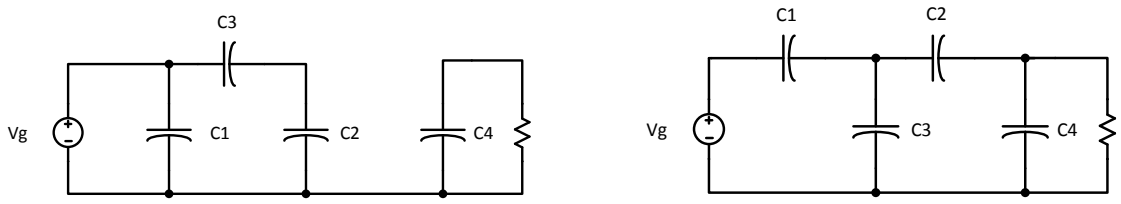


Figure 3.4: Simplified 5/1 up converter

The converters with higher number of elements require a more organized approach. The Kirchoff's voltage equations remain the same but are written in an organized matrix form. Both [62] and [63] include methods to analyze SC converters. In [62] all the capacitor voltages are used in calculation, which is suitable for the topological generation. However to find all the capacitor voltages only tree voltages are necessary as outlined in [63]. Therefore for simplicity tree voltages method will be explained, but both can be used to solve the equations for voltages across all capacitors.

The example converter with 4 capacitors and an ideal conversion ratio of 5 is given in Fig 3.4. In the given converter, capacitors are arranged in a way that each capacitor adds another input voltage level to the final output. The operation of the converter can be explained intuitively by iterating between the phases. During phase 1 C_1 is charged to the input voltage, which forces C_3 to be charged to twice the input voltage during phase 2. Going back to phase 1 it can be followed that $V_g + V_{C_3} = 3 \times V_g$ which is the voltage across C_2. Finally in phase 2 the C_4 is charged to $V_g + V_{C_1} + V_{C_2} = 5 \times V_g$. While this method provides insight on how SC converters work and designed, it is not suitable for performance analysis and modeling and as explained in [62] some topologies are not as straightforward as others.



(a) (b)

Figure 3.5: 2 phases of a 5/1 up converter

First step of the analysis is selecting a tree (network that reaches every not but has no loops). For the converter under consideration V_g, C_3, C_4 reaches all the nodes in both phases and forms no loops. The graph sections related to V_g, C_3, C_4 are called twigs, since they are parts of the tree. Remaining elements are called link elements, because when they are included a loop is formed. In an SC converter with k number of capacitors, k independent equations are needed to solve the voltages across capacitors in terms of input voltage. Of the k capacitors k_l are link elements and k_t are twigs. Since including a single link element completes a loop, it can be said that in each KVL equation there has to be a single link element. So the link elements in each phase can be represented as an identity matrix with relative twigs and the input voltage is added to the equation. This approach yields a matrix for the phase 1 as shown in equation 3.4.

$$B_{f1} = \begin{pmatrix} U_{(2,2)} & B_{(2,2)} & b_{(2,1)} \end{pmatrix} \tag{3.4}$$

B_{f1} represents the matrix that holds the loop equations for the first phase. The $U_{(2,2)}$ is the identity matrix representing the link elements in each loop. The $B_{(2,2)}$ is the matrix that has coefficients used for twigs in each loop. The $b_{(2,1)}$ is the vector that has the coefficients for the input voltage in each loop. A similar matrix can also be formed for the phase 2 as well with the same form but named B_{f2}. Finally, these two matrices can be combined as in equation 3.5.

$$\begin{pmatrix} U_{(2,2)} & B1_{(2,2)} & b1_{(2,1)} \\ U_{(2,2)} & B2_{(2,2)} & b2_{(2,1)} \end{pmatrix} \begin{pmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_g \end{pmatrix} = 0 \tag{3.5}$$

One important result from equation 3.5 is that the first two rows and the second two rows have the same coefficients for the link elements. Therefore it is possible to subtract the first part from the second and solve a matrix that is smaller but in doing so the voltage information about the link elements are lost. However from circuit analysis it is known that all the voltages in a circuit can be written as twig voltages, meaning as long as voltages of link elements are needed explicitly there is no need to calculate them. The resulting matrix from the subtraction is given in equation 3.6.

$$\begin{pmatrix} B1_{(2,2)} - B2_{(2,2)} & b1_{(2,1)} - b2_{(2,1)} \end{pmatrix} \begin{pmatrix} V_{C3} \\ V_{C4} \\ V_g \end{pmatrix} = 0 \tag{3.6}$$

With the tree selected for the example in Fig 3.4, the matrix in equation 3.7 is obtained through KVL equations.

$$\begin{pmatrix} 1 & 0 & \vdots & 0 & 0 & \vdots & -1 \\ 0 & 1 & \vdots & -1 & 0 & \vdots & -1 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 1 & 0 & \vdots & -1 & 0 & \vdots & 1 \\ 0 & 1 & \vdots & 1 & -1 & \vdots & 0 \end{pmatrix} \begin{pmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_g \end{pmatrix} = 0 \tag{3.7}$$

The matrix calculated from equation 3.7 that follows the usage in equation 3.6 is given in equation 3.8.

$$\begin{pmatrix} 1 & 0 & \vdots & -2 \\ -2 & 1 & \vdots & -1 \end{pmatrix} \begin{pmatrix} V_{C3} \\ V_{C4} \\ V_g \end{pmatrix} = 0 \tag{3.8}$$

And finally the equation 3.8 can be solved by following equation 3.9.

$$\begin{pmatrix} V_{C3} \\ V_{C4} \end{pmatrix} = -(B1_{(2,2)} - B2_{(2,2)})^{-1}(b1_{(2,1)} - b2_{(2,1)})V_g \tag{3.9}$$

Once solved, the equation 3.9 yields the vector $[2, 5]$ which means that the voltage across C_3 is 2 times the input voltage and voltage across C_4 is 5 times the input voltage.

Using this method all types of converters can be analyzed for their ideal conversion ratios. However this method has to be expanded to cover the under load conditions and dynamic considerations.

3.2.2 Charge Transfer in a 1/1 Converter

A 1/1 converter operates in two phases, as shown in Fig. 3.6. During phase 1 $P1$, the flying capacitor charges to the input voltage V_i and during phase 2 $P2$, this capacitor discharges to output voltage V_o. If no load is present at the output, the output voltage becomes equal to the input voltage at the steady state (*i.e.*, V_o=V_i. The charge transfer characteristics of each phase are investigated in this section.

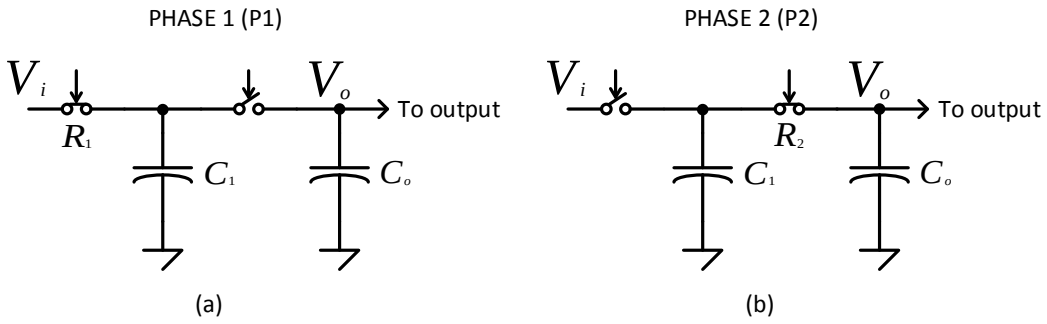


Figure 3.6: Two phases of operation for a 1/1 SC converter; (a) phase 1 (charging phase) and (b) phase 2 (discharging phase).

R_1, C_1, C_o represent, respectively, the on-resistance of the switch between the input source and the top plate of the capacitor, flying capacitor, and output capacitor, as shown in Fig. 3.6a. The time domain expressions of this phase can be written as

$$V_{C_1(t)} = (V_i - V_{C_1(0)})(1 - e^{\frac{-t}{R_1 C_1}}) + V_{C_1(0)} \tag{3.10}$$

where $V_{C_1(0)}$ is the initial voltage on C_1 and t is time. At the end of $P1$, (3.10) becomes

$$V_{C_1(1)} = (V_i - V_{C_1(0)})(1 - e^{\frac{-D_1 T}{R_1 C_1}}) + V_{C_1(0)} \tag{3.11}$$

where $V_{C_1(1)}$ denotes the voltage of C_1 at the end of $P1$, D_1 represents the duty cycle, and T is the period of the input switching signal.

The equivalent circuit during $P2$ is illustrated in Fig. 3.6b where R_2 represents the on-resistance of the switch between the output and top plate of the capacitor. Using Kirchoff's current law (KCL) and KVL for the equivalent circuit, the current and voltage con be written as

$$\text{KCL: } i_{C_1} + i_{C_o} + i_o = 0 \tag{3.12}$$

$$\text{KVL: } V_{C_1} + V_{R_2} = V_o \tag{3.13}$$

where i_{C_1}, i_{C_o} and i_o are, respectively, the current from C_1, current from C_o, and output current. By considering the voltage/current relationship of the capacitors, (3.12) can be written as

$$C_1\frac{dV_{C_1}}{dt} + C_o\frac{V_{C_o}}{dt} + i_o = 0 \tag{3.14}$$

By substituting (3.13) into (3.14), KCL can be written as

$$C_1\frac{dV_{C_1}}{dt} + C_o\frac{d(V_{C1} + R_2C_1\frac{dV_{C1}}{dt})}{dt} + i_o = 0 \tag{3.15}$$

and after simplifications

$$R_2C_oC_1\frac{d^2V_{C_1}}{dt^2} + (C_1 + C_o)\frac{dV_{C1}}{dt} + i_o = 0. \tag{3.16}$$

The solution of (3.16) can be written as

$$V_{C_1(t)} = k_1\frac{R_2C_oC_1}{C_1 + C_o}e^{-(\frac{(C_1+C_o)}{R_2C_oC_1}t)} - \frac{i_o}{C_1 + C_o} + k_2 \tag{3.17}$$

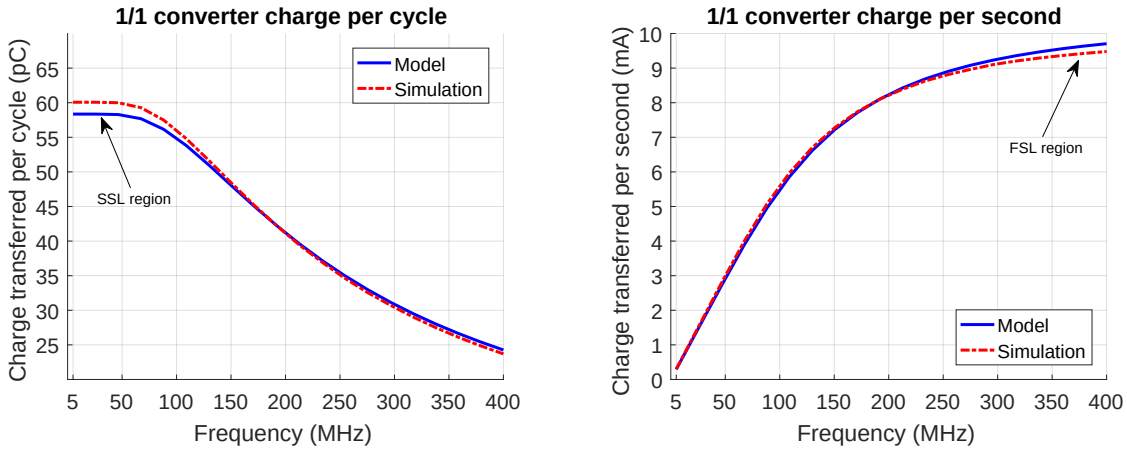
where k_1 and k_2 are the constants that are obtained from the boundary conditions. The voltage of the capacitor at the end of $P1$ should be the same at the beginning of $P2$ as

$$V_{C_1(t=0)} = V_{C_1(1)} \tag{3.18}$$

where $t = 0$ is the point when V_{C_1} is equal to its voltage at the end of the previous phase.

$$V_{C_1(t=\infty)} = \frac{V_{C_1(1)}C_1 + V_{o(1)}C_o}{C_1 + C_o} \tag{3.19}$$

where $t = \infty$ defines the point when V_{C_1} is equal to a value that can be obtained with perfect charge sharing between two capacitors minus the leakage due to the output current. Based on (3.18) and



(a) (b)

Figure 3.7: Charge transfer comparison in a 1/1 SC converter over 5-400 MHz frequency range between the model and the simulation; (a) per cycle charge transfer (b) per second charge transfer

(3.19), k_1 and k_2 can be written as

$$k_1 = \frac{V_{C_1(1)}C_o - V_{o(1)}C_o}{R_2 C_o C_1} \tag{3.20}$$

$$k_2 = \frac{V_{C_1(1)}C_1 + V_{o(1)} + C_o}{C_1 + C_o} \tag{3.21}$$

where $V_{o(1)}$ is the final output voltage from the previous phase ($P1$). At the end of $P2$, the voltage on the capacitor becomes

$$V_{C_1(2)} = k_1 \frac{R_2 C_o C_1}{C_1 + C_o} e^{-(\frac{(C_1+C_o)}{R_2 C_o C_1} D_2 T)} - \frac{i_o}{C_1 + C_o} + k_2 \tag{3.22}$$

where D_2 is the duty cycle of the second phase. Using (3.11) and (3.22), a 1/1 converter can be modeled for (i) the charge transferred to the output per cycle by using $(V_{C1(2)} - V_{C1(1)}) \times C_1$ and for (ii) the charge transferred to the output per second (output current) by using $\frac{(V_{C1(2)} - V_{C1(1)}) \times C_1}{T}$.

The charge transfer rate depends on the output voltage, frequency, resistance of switches, capacitor value, and duty cycle, as explained in (3.11)-(3.22). The frequency, resistance, capacitor value, and duty cycle can therefore be used to regulate the charge transfer to the output hence controlling the output voltage, as illustrated in Fig. 3.3.

To validate the results of the analysis, first, the charge transfer to grounded (0 V at the output) output from the model and the results from the simulation with its equivalent circuit are compared. For this comparison, an SC converter is used with a 60 pF of total flying capacitor, 50Ω resistors in each phase, and an 800 pF decoupling capacitor. The converter operates at 50% duty cycle with varying frequencies where the input voltage V_i is 1V. The converter's operating frequency is swept between 5 MHz and 400 MHz to clearly demonstrate the slow switching limit (SSL) and fast switching limit (FSL) characteristics [63]. The results from the model are obtained using (3.11) and (3.22), and the simulation results are obtained using linear resistance switches (*i.e.*, constant on and off resistance over different voltages) and ideal capacitors. The comparison of the charge transfer per cycle between the model and the simulation results obtained by using the aforementioned converter is shown in Fig. 3.7a. Note that the amount of transferred charge per cycle stays constant up to 50 MHz and then starts dropping. The region where the charge transfer per cycle remains constant is the SSL region. In this SSL region, the capacitors charge and discharge close to their final voltages in a given configuration in each phase. Therefore in this region, the charge transfer per cycle remains constant regardless of the frequency since the capacitor charge sharing reaches the equilibrium. As the frequency increases, the RC time constant formed by the capacitor and switch resistance becomes comparable to the period and therefore the amount of charge transfer per cycle drops, causing the converter to enter the FSL region. As seen from Fig. 3.7a, the analytic model follows both the SSL and FSL behaviors accurately. Root mean square error of the model as compared to the simulations is 2.09%. The error is primarily due to the finite rise/fall transition times in the simulations and the accumulated error due to the calculation of the charge using integration in the simulations. The amount of charge transfer per second is shown in Fig. 3.7b. Note that the charge transfer per second is actually the output current. In the SSL region, the increase in the output current is linear as the charge transfer per cycle is relatively constant. However, this behavior changes when the charge transfer per cycle starts to drop because of the incomplete charging of capacitors. Again, the analytic model follows both the SSL and FSL behaviors accurately with 1.59% root mean square error.

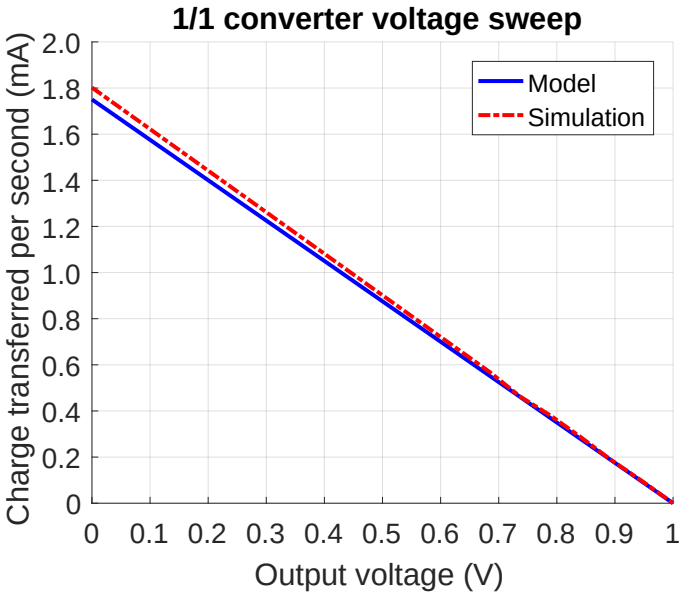


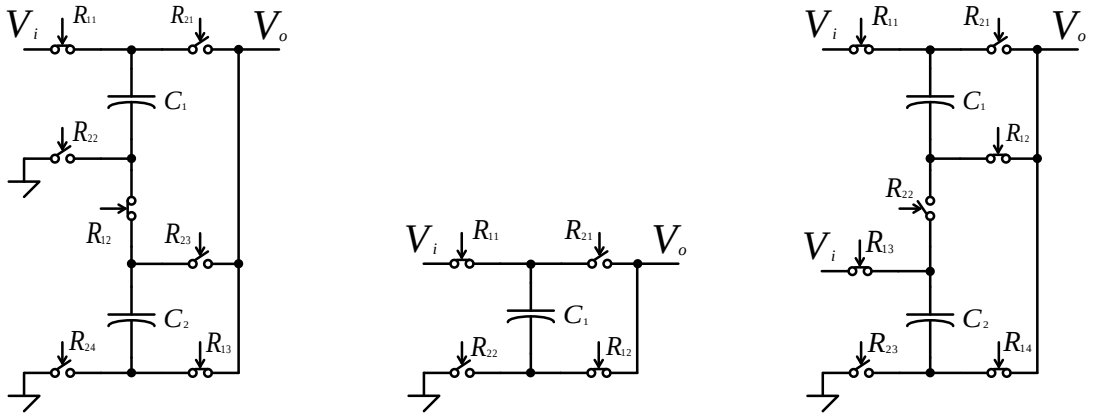
Figure 3.8: Per second charge transfer comparison in a 1/1 SC converter over 0 to 1 V output voltage range between the model and the simulation.

Another metric that needs to be validated in the model is the behavior of the output current over a range of output voltages to evaluate the transient performance at different output voltages. This comparison between the model and simulation at 30 MHz (inside SSL region) frequency with varying output voltage is shown in Fig. 3.8. A linear drop over output voltage can be observed from these results. The primary reason for this behavior is because the charge transferred to the output is given as $(V_{C1(2)} - V_{C1(1)}) \times C_1$ and as given in (3.11) and (3.22), $V_{C1(1)}$ and $V_{C1(2)}$ have a linear relation with the output voltage. The analytic model follows the same behavior with 2% root mean square error.

The developed analytic model follows the expected behavior and provides a mathematical basis on how a 1/1 SC converter is affected by its operating parameters. In the following subsection this model is extended to cover different conversion ratios.

3.2.3 Charge Transfer in an m to n Converter

In order to implement conversion ratios other than 1, 2, 1/2 and -1, more than one flying capacitor is needed [62, 63], making the explicit analysis of the charge transfer complicated due



(a) (b) (c)

Figure 3.9: Different SC converter topologies with abstract switches that can be implemented in a reconfigurable converter; a) 1/3 converter, b) 1/2 converter, and c) 2/3 converter.

to the additional nodes in the system equations. A method to simplify the analysis of converters with different ratios is needed. According to the analysis in [63, 68], the charging and discharging behavior of individual capacitors can be represented with a charge transfer vector. This vector includes the information on the charge transfer that occurs in each capacitor in each period that is normalized to the charge transferred to the output. The output resistance of a given configuration at SSL is determined both by this charge transfer vector and by the fundamental loop equations. Based on the analysis provided in [63, 68], the charge transfer rate at SSL for any configuration can be normalized to any other configuration since the charge transfer vectors are determined by the topology of the converters.Similarly, at FSL, the converter behavior is determined by the charge transfer vectors which is also affected by the on resistance of the switches [68]. The behavior at FSL can also be normalized to a 1/1 converter with a multiplier as long as the equivalent resistances are kept the same to guarantee the same time constant. The charge transfer characteristics of an optimized SC converter – regardless of the conversion ratio and operating conditions – can therefore be normalized to a 1/1 converter.

To use the model of a 1/1 converter to any converter at SSL over a range of output voltages, an analysis of the charge transfer of the SC converters is performed at the point where the charge

transfer in each phase is complete. The first condition that is investigated at SSL is when the output voltage is kept at zero. The output charge transfer characteristic under zero output voltage provides insight on how the charge transfer in each conversion ratio is performed relative to the other conversion ratios.

The operation of a 1/3 converter is shown in Fig. 3.9a. If V_o is kept at zero, both C_1 and C_2 are discharged to zero during $P2$. Since V_o is equal to zero during $P1$, C_1 and C_2 are charged to $V_i/2$ when both capacitors are equal to $C_{unit}/2$. The charge transfer during $P1$ results in $\frac{V_i}{2} \times C_{unit}$ amount of charge to transfer to the output. At the beginning of $P2$, both capacitors will discharge from $\frac{V_i}{2}$ to 0 while delivering $C_{unit} \times V_i$ amount of charge to the output. The total charge that is delivered to the output in a 1/3 configuration can be summed as $0.75 \times C_{unit} \times V_i$ per cycle where C_{unit} is the unit capacitor that is equal to the sum of C_1 and C_2.

The operation of a 1/2 converter is shown in Fig. 3.9b. If V_o is kept at zero, in $P2$, the capacitor C_1 charges to V_i while delivering $C_1 \times V_i$ amount of charge to the output. In $P1$, the capacitor C_1, that was previously charged to V_i, is discharged to ground while transferring $C_1 \times V_i$ amount of charge to the output. Since the reconfigurable converter is implemented using the same capacitors, the total capacitor is assumed to remain the same between conversion ratios For example, the C_1 in a 1/2 converter is equal to C_{unit}. In total, a 1/2 converter delivers $2 \times C_{unit} \times V_i$ amount of charge to the output per cycle.

The last conversion ratio that can be implemented using two capacitors is the 2/3 converter, as illustrated in Fig. 3.9c. The capacitors C_1 and C_2 in a 2/3 converter are charged to V_i during $P1$ if V_o is zero. During $P1$, assuming both C_1 and C_2 are equal, $C_{unit} \times V_i$ amount of charge is delivered to the output. During $P2$, both C_1 and C_2 are discharged to ground in a series connection configuration while delivering $C_{unit}/2 \times V_i$ amount of charge to the output, in total delivering $1.5 \times C_{unit} \times V_i$ amount of charge in a single cycle.

The second condition that will be investigated at SSL is the condition where there is no charge transferred to the output. As analyzed in [8], zero charge transfer occurs when the output voltage is equal to $V_i \times$ ICR where ICR is the ideal conversion ratio of the given SC converter topology. For example, a 1/2 converter delivers no charge to the output if the output voltage is

Table 3.1: Comparison of Charge Transfer in Different Configurations

Ratio	Charge transfer at $V_o = 0$	V_o for zero charge transfer
1/1	$V_i \times C_{unit}$	V_i
1/3	$0.75 \times V_i \times C_{unit}$	$V_i/3$
1/2	$2 \times V_i \times C_{unit}$	$V_i/2$
2/3	$1.5 \times V_i \times C_{unit}$	$2V_i/3$

equal to $V_i/2$ because under this condition, the charge difference on the flying capacitor between two phases becomes zero. The charge transferred to the output per cycle at zero output voltage and the output voltage at which the charge transferred to output per cycle becomes zero for several conversion ratios of interest are given in Table 3.1.

As the charge transfer per cycle at two different output voltages is known, the curve that characterize the charge transfer over varying output voltages can be written as

$$Q_{o_{mn}} = Q_{o_{11}} \times c_{mn} \times (1 - \frac{V_o}{V_i \times \text{ICR}}) \tag{3.23}$$

where $Q_{o_{mn}}$ is the charge transfer per cycle for an n/m converter, $Q_{o_{11}}$ is the charge transfer per cycle for a 1/1 converter, c_{mn} is the multiplier that represents the ratio of charge being delivered to the output with respect to a 1/1 converter at 0 V output voltage, as listed in Table 3.1, and ICR is the ideal conversion ratio $\frac{n}{m}$. In (3.23), $Q_{o_{11}}$ is calculated from (3.11), (3.22) and using $(V_{C1(2)} - V_{C1(1)}) \times C_1$. To make sure that the (3.23) holds true at FSL, the total resistance in the charge transfer path in each phase of an n/m converter should be equal to the corresponding phase's total resistance in a 1/1 converter used in (3.11) and (3.22). The total capacitor value should also be the same. For example, in a 1/3 converter, two capacitors C_1 and C_2 have to satisfy $C_1 + C_2 = C_{unit}$ where C_{unit} is the capacitor value in a 1/1 converter. Similarly, the resistances need to follow the same principle. For example, the sum $R_{11} + R_{12} + R_{13}$ in a 1/3 converter should be equal to R_1 of a 1/1 converter. In reconfigurable converters, the values of capacitors and switch resistances of each conversion ratio may differ from the examples given here based on how the different conversion ratios are implemented. However, the proposed model is scalable such that the resistance values in

the original 1/1 model ($R_1, R2$) can be modified according to the new conversion ratio to address the difference.

To validate (3.23), 1/1, 1/3, 1/2, and 2/3 converters, which have the same total capacitor and same total resistance values during each phase of the operation, are simulated and compared with the mathematical model. The charge transfer rates calculated from the model and obtained from the simulations for the given conversion ratios are shown in Fig. 3.10. With the aforementioned modification to (3.23), the results for the charge transfer per cycle and per second (output current) align well with less than 3% error. Note that the c_{mn} parameter also multiplies the error for both sweeps. Even the small errors in the original 1/1 model therefore may become important especially in the output current and output voltage relation, as shown in Fig 3.10c, Fig 3.10f and Fig 3.10i.

The generalized models developed in this section are used to provide an understanding for how the transient behavior of reconfigurable SC converters are affected when the conversion ratio changes. Additionally, this analysis simplifies the linearization of different converter types and can potentially be used to optimize the control loop characteristics.

3.3 Transient Response Time Implications on Reconfigurable or Response-Enhanced Converters

As the analysis in the previous section mathematically demonstrates, the charge transfer rate strongly depends on the conversion ratio, the instantaneous output voltage, and the parameters that are used in the control[1]. When a reconfigurable converter is used, the dependency of the charge transfer rate on the output voltage and the conversion ratio may cause sudden increases or drops in charge transfer rate at the boundary conditions of different configurations due to the lack of a stepped transition between conversion ratios. For example, when a converter is reconfigured from 1/2 to a 2/3 configuration to set the output voltage to a higher level, a sudden increase in the charge transfer rate occurs. This increase in charge transfer rate may be acceptable and even beneficial in an unregulated open loop voltage converter as the increase in charge transfer rate will speed up the

[1]Although frequency control is used in our analysis, other control techniques based on the duty cycle, resistance, and capacitance can be used similarly.

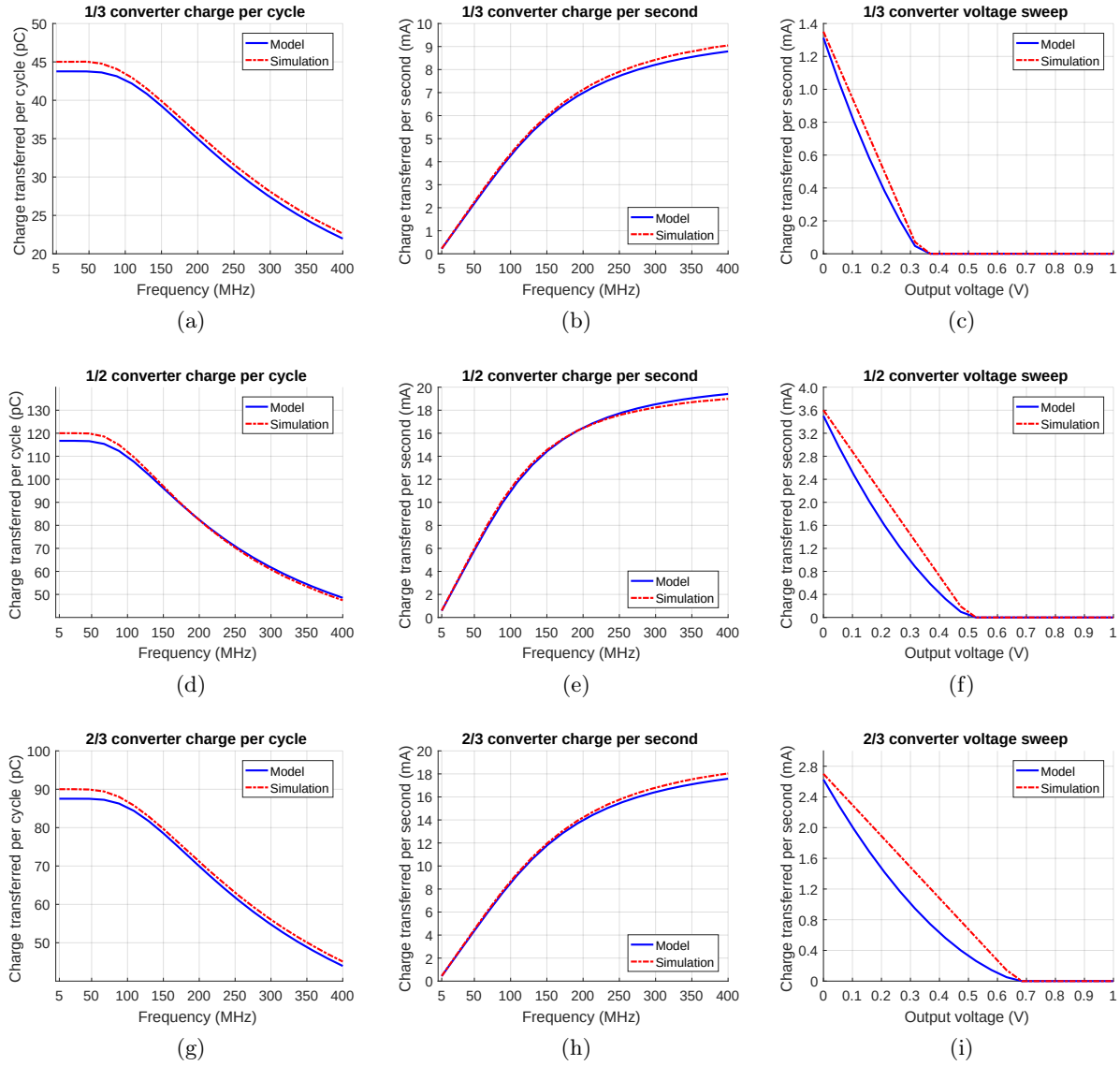


Figure 3.10: Comparison of charge transfer between the generalized model and the simulation in converters with different conversion ratios; (a), (d), (g) per cycle transfer for 1/3, 1/2, and 2/3 converters over 5-400 MHz frequency range, (b), (e), (h) per second transfer for 1/3, 1/2, and 2/3 converters over 5-400 MHz frequency range, (c), (f), (i) per second transfer for 1/3, 1/2, and 2/3 converters over 0-1 V output voltage range.

settling. However, when the output voltage is controlled within a loop, a sudden increase means that the control loop needs to take enough samples with the new configuration to settle at the correct value. Moreover, to be able to deliver the same amount of current close to its highest output voltage, an SC converter configured as a 1/2 converter needs to operate at the highest possible

frequency while a 2/3 configuration delivers the highest amount of current at the switching point and needs to operate at the lowest possible frequency. This means that the control signal has to swing from one end to the other which – in most integrator-comparator based control loops – may cause a significant overshoot as the integrator does not settle before taking sufficient number of samples. The same concept can be applied to a converter that is reconfigured from 2/3 to 1/2 configuration, however, in this case, the reconfiguration will cause an undershoot.

The transient response enhancement techniques proposed in [49, 57, 66] also suffer from a similar problem. The response enhancement is typically implemented by adding an interrupt state which is triggered when there is an extreme voltage drop at the output. Based on the output voltage, one of the control parameters of the SC voltage converter is set to a higher level to speed up the transient recovery. For example, in [49], the frequency is set to the highest level when there is a voltage drop at the output. However, setting the control parameter to the highest possible value causes the same issue observed in the reconfigurable converters due to a sudden increase in the charge transfer rate. This may cause an integrator-comparator based control loop to swing between the interrupt state and the regular operation, leading to a hysteresis condition. Additionally, the comparator that triggers this interrupt state has to have a reference and if this reference voltage is generated from the original reference voltage, the interrupt state may be triggered during reconfiguration when reference voltage is changed, potentially causing issues when the fast response is needed for DVS.

3.3.1 In Reconfigurable Converters

A reconfigurable converter similar to [65] that has 1/1, 2/3, 1/2, 1/3 ratios is investigated in this section because these conversion ratios cover most of the range that is viable for DVS and can be implemented using only two capacitors. The architecture of the converter that is analyzed is given in Fig. 3.11. A frequency based control loop, a converter with lossless capacitors, and switches with linear resistances are used in the analysis. The ratios that are being used are selected based on the desired output voltage to provide the maximum efficiency over the total output voltage range. Since the model used in this work does not contain information about the losses and efficiency of

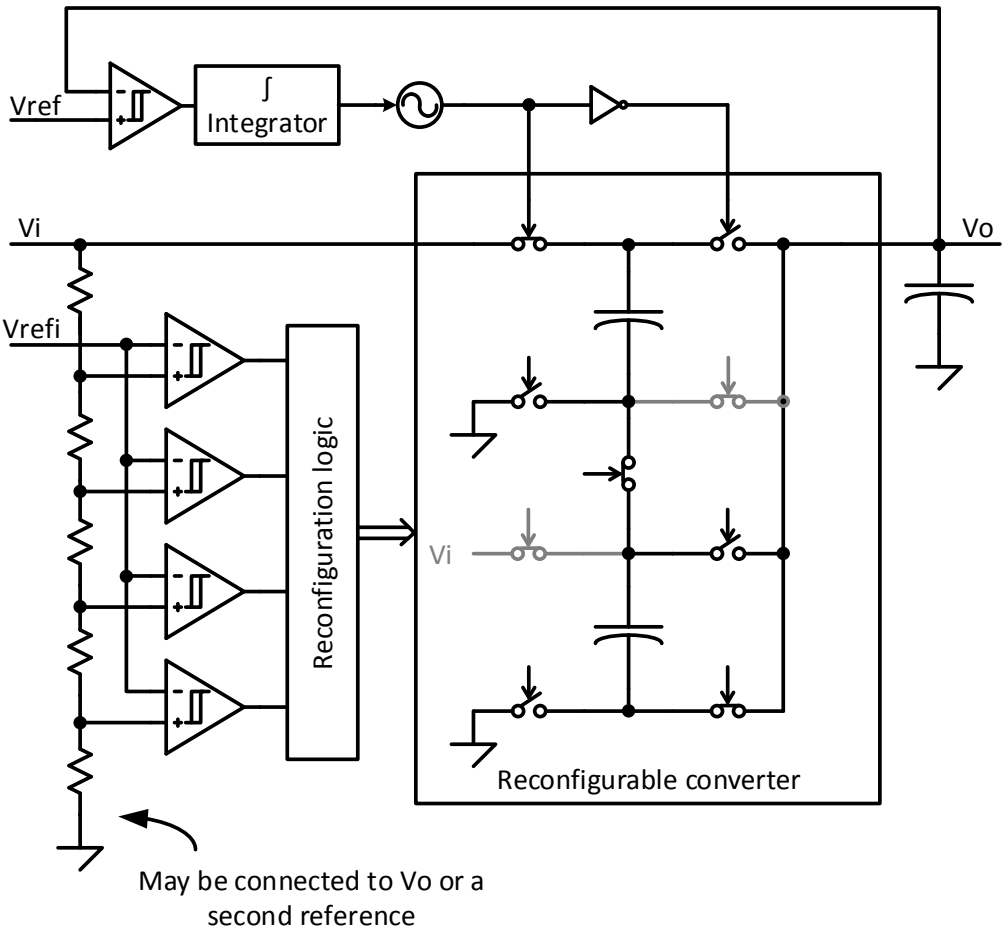


Figure 3.11: A reconfigurable SC converter with a conventional control loop and reconfiguration logic. The black switches are active during 1/3 conversion, whereas gray switches are inactive for 1/3 conversion. Different conversion ratios are implemented by reconfiguring the active and passive switches.

the converter, the regions of operation for each conversion ratio are chosen as scaled versions of the operating regions proposed in [65]. Finally, without losing generality, the input voltage of 1 V will be used to simplify the analysis which may result in unrealistically small output voltages but can be scaled up in a practical design.

A reconfigurable converter with a frequency based control that operates in the 1/3 configuration for the output voltage range from 0 V to 0.25 V, while the 1/2, 2/3 and 1/1 configurations, respectively, covering the 0.25 V - 0.45 V, 0.45 V - 0.61 V, 0.61 V - 1 V ranges is investigated in

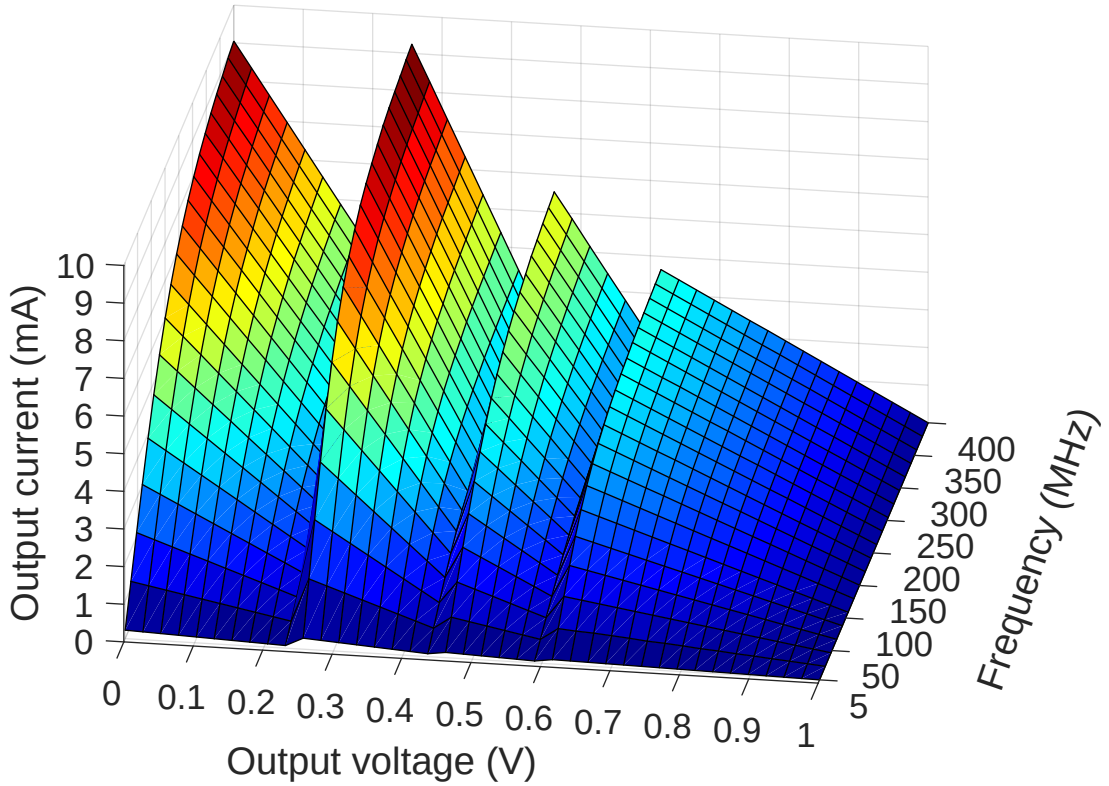


Figure 3.12: Output current (charge transfer per second) of a reconfigurable SC converter that is reconfigured to maintain high efficiency over 0 to 1 V output voltage range.

this section. The reconfigurable converter has a 60 pF total flying capacitor divided into two 30 pF capacitors to implement different conversion ratios, 50 Ω equivalent switch resistance in each phase of all conversion ratios, and a 800 pF decoupling capacitor. When the analysis from the previous section is applied to the reconfigurable converter with the given characteristics, the output current distribution over output voltage and the operating frequency given in Fig. 3.12 is obtained. As the output current in (3.11) and (3.22), and the corresponding transformations for different conversion ratios depend on the instantaneous voltage, sudden increases or drops in the output current between boundary conditions can be observed in Fig. 3.12. To determine how a sudden increase in the output current affects the control parameter, which is the frequency in this case, the optimal frequency of the operation to maintain a constant output current at different output voltages can be investigated, as shown in Fig. 3.13. To deliver 2 mA output current, a 1/3 converter needs to start operating

at 50 MHz and at the end of the possible output voltage range, the converter needs to operate at 171 MHz frequency to keep up with 2 mA output current because of the dependence of the charge transfer rate on the output voltage. At 0.25 V output voltage, using a 1/3 converter is no longer viable due to the significant degradation in the power efficiency [65]. When a 1/2 configuration is enabled at this boundary condition, an operating frequency of 25.8 MHz is needed to deliver 2 mA to the output. However, the value held in the integrator cannot transition from the optimum boundary values for 1/3 and 1/2 configurations instantaneously in a control loop because of the nature of the control loop (see Fig. 3.11). As a result, when the reference voltage of the converter is changed in a sufficiently large step, causing the converter to be reconfigured to a different conversion ratio, the converter keeps delivering a larger amount of charge than what is required to maintain the desired output voltage until the integrator takes sufficient number of samples to accurately follow the output current of the new configuration.

To simulate this behavior, a control loop is modeled in verilogA. The controller includes a 9-bit (512 levels) integrator, a 9-bit digitally controlled oscillator (DCO), and a logical statement which decides if the integrator value should be increased, decreased, or kept constant. To prevent a hysteresis condition between different levels, the control loop keeps the integrator value constant when the output voltage is within 10 mV of the reference voltage. The response of the converter is simulated in conjunction with the control loop modeled in verilogA that is stimulated by a reference voltage step from 200 mV to 350 mV and by a reference voltage step from 200 mV to 260 mV. The simulation results of this converter while driving a 75 Ω output load is shown in Fig. 3.14. The transition from 200 mV to any voltage above 250 mV causes a reconfiguration which is a reconfiguration from a 1/3 converter to a 1/2 converter in the case of Fig. 3.14. When the target voltage is 350 mV, the control loop adjusts to this voltage in 50 ns since this voltage is close to what can be achieved using the same integrator value. However, when the step is close to the starting point of the operating range of the next configuration, which is 1/2 in this case, the control loop needs to get more samples with the new reference voltage and the new configuration. This causes a significant increase in the response time as shown in Fig. 3.14 which takes 1.15 μs to reach the target voltage.

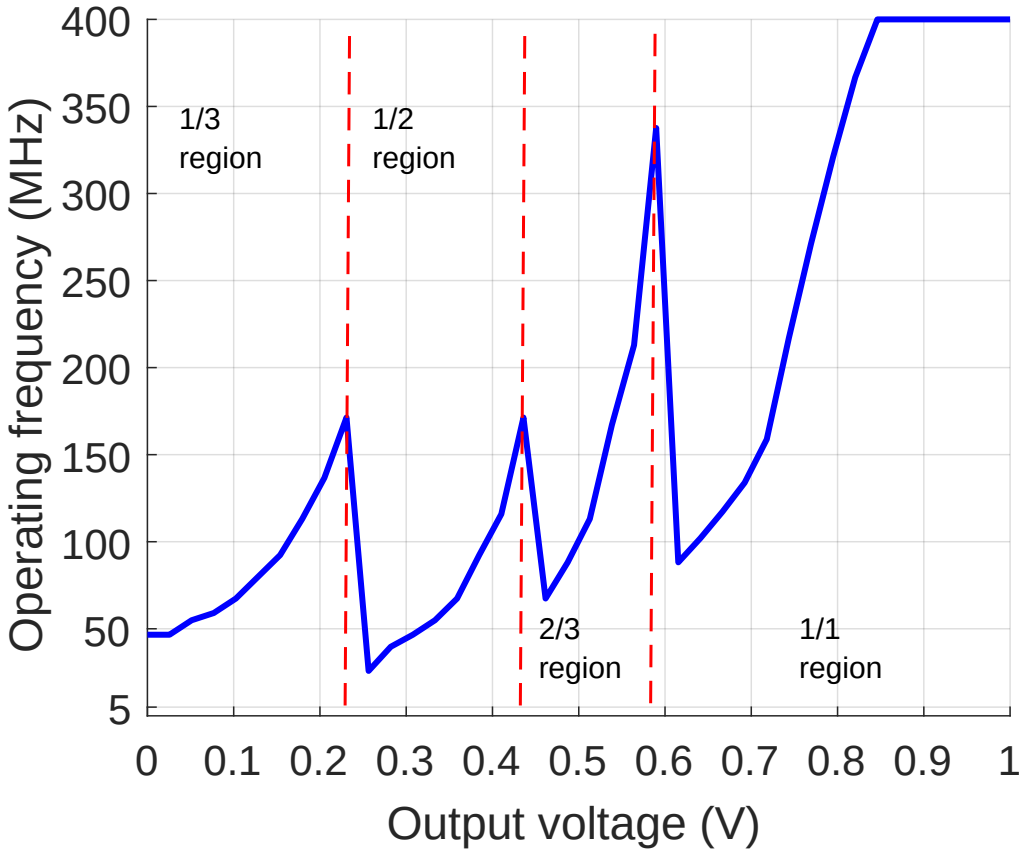


Figure 3.13: Operating frequency required for the modeled reconfigurable converter over 0-1 V output voltage to maintain 2 mA output current. Notice that a 1/1 converter cannot maintain 2 mA when the output voltage exceeds 0.85 V and therefore it stays at the maximum frequency. After every reconfiguration, converter needs to change its operating frequency drastically to maintain a constant current over different output voltages.

The effect shown in this section has two implications i) if no precaution is taken, the settling time will be longer for specific steps while being significantly shorter for others reducing the maximum DVS frequency and ii) if the conversion ratio is being determined in an additional loop that has a dependence on input, output, and reference voltages, the overshoot in the output voltage waveform may cause a second unintended reconfiguration that may cause longer settling times or even instability.

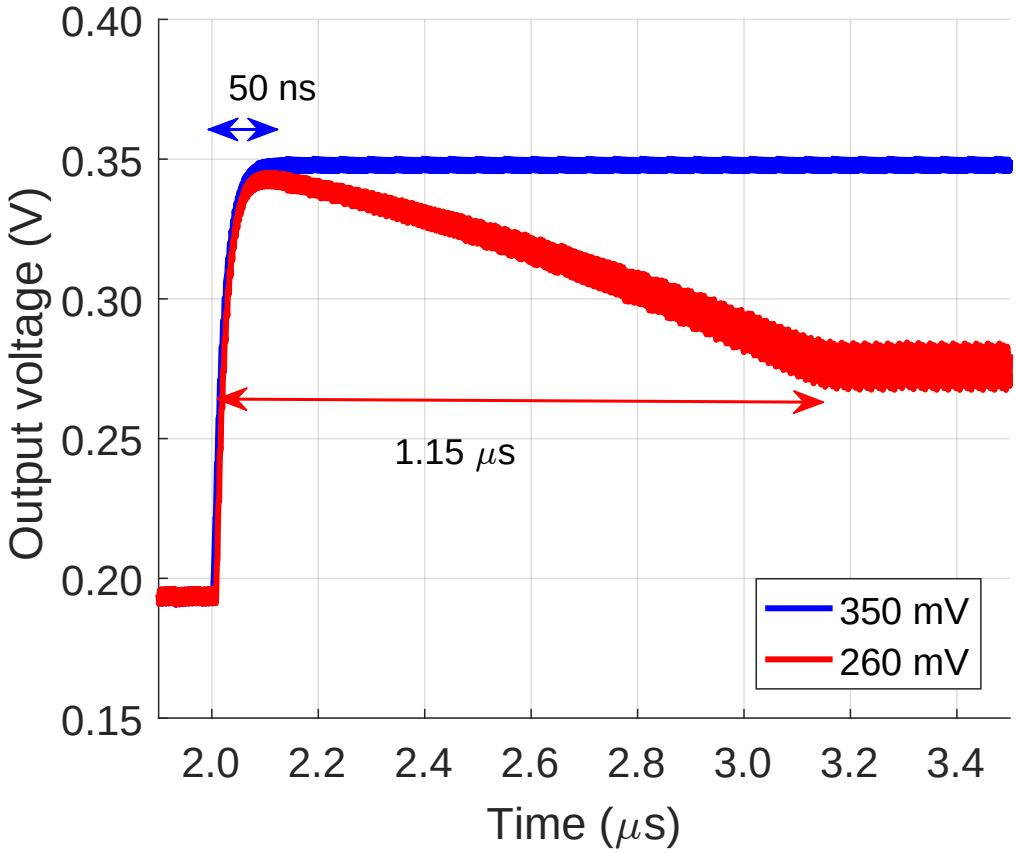


Figure 3.14: Transient response of a reconfigurable converter with a conventional control loop given in Fig. 3.11 to a voltage reference step from 210 mV to 350 mV and a voltage reference step from 210 mV to 260 mV. Notice that both steps require converter to be reconfigured from 1/3 configuration to 1/2 configuration.

3.3.2 In Response-Enhanced Converters

SC converters with response-enhancement features may also be susceptible to a similar disparity between the integrator value and the actual output resistance [49, 57, 66]. For example, in [49], an interrupt state is triggered when there is a large voltage drop at the output. During this interrupt state, the parameter that controls the charge transfer rate is set to the maximum value to speed up the charge recovery. Using this kind of transient recovery method with a fast comparator improves the transient recovery during large transients (*i.e.* 0 to max output current) because the final value that the integrator will need to settle is close to the maximum value. However, during smaller transients at the load current or at the reference voltage, the transient recovery loop may

be triggered and the converter parameters may change, drastically increasing the settling time. Alternatively, in [57, 66] the voltage conversion ratio of a reconfigurable converter is changed to reduce the response time. While changing the conversion ratio indeed increases the charge transfer rate, it may also cause disparity between the value held in the integrator and the actual charge transfer rate. Therefore, in the next subsections, both of these techniques which utilize interrupt states and conversion ratio manipulation are investigated for their susceptibility.

3.3.2.1 Enhancing the Response with Interrupt States

In this type of response time improvement, typically, an additional comparator that is triggered at a slightly lower voltage than the reference voltage is used to sense a voltage drop. When the additional comparator senses a large voltage drop, the control circuit is given the signal to increase the charge transfer to the output by setting its control parameter (*i.e.*, frequency) to its highest value. While this type of enhancement is typically designed to only respond to large transient spikes at the load, it is also possible to trigger this type of system with smaller steps under certain conditions. For example, the system given in [49] may not be able to distinguish the transient at the output from an increase in the reference voltage depending on how the reference voltage for the enhancement loop is generated. In this case even though the stepped up reference voltage is close to the original reference voltage, the enhancement loop may become active and cause a steep increase in the charge transfer rate. Additionally, certain process and mismatch errors in the comparators may also cause the enhancement loop to become active with a smaller transient signal, and may have a similar effect.

A verilogA model of 9-bit digital control loop is used for the simulations which sets the integrator value to its maximum when the output voltage drop is higher than 30 mV compared to the reference voltage. The same converter used to verify the models is used in the simulations of the transient enhancement. However this converter operates only in the 1/3 configuration (*i.e.* not reconfigurable) with 210 mV constant voltage reference. In this case the load resistance is set to 100 Ω to reduce the DC current and better focus on the effects of the transient current. The output voltage is shown in Fig. 3.15 when additional current sources that step up from 0 to 650 μA and

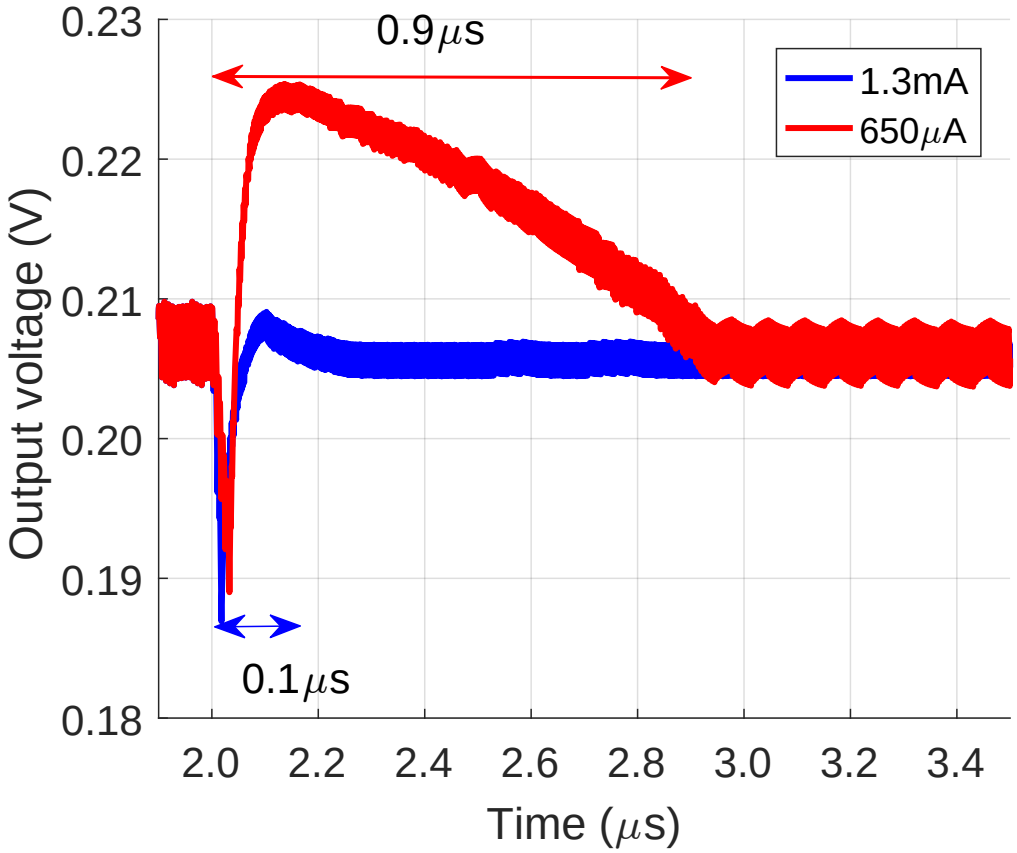


Figure 3.15: Transient response of a 1/3 converter with a loop and an interrupt state that sets the control parameter to the maximum value when the output voltage drops more than 30 mV. Two different current pulses of 1.3 mA and 650 μA are used to trigger the interrupt state. Notice that when triggered by a smaller pulse, the output voltage first spikes up because of the manipulation of the control parameters.

from 0 to 1.3 mA and 650 μA are individually applied to the output. Under a large step of 1.3 mA, the output recovers from the transient in 100 ns. When a smaller step triggers the same interrupt state, the voltage overshoots and slowly converges to the reference voltage. The reason for the slow response is that the integrator is set to the highest value and does not house a fast recovery scheme to get back to correct value. Even in the case that smaller load steps are considered in the design, this additional loop may also get triggered by a change in the reference voltage which may affect the performance of a DVS system.

3.3.2.2 Enhancing Response with Conversion Ratio Manipulation

Changing the conversion ratio is an alternative way to improve the response time of SC converters [57, 66]. A secondary loop comparing the input voltage, output voltage, or the difference between the input and output voltage can be used to determine when to change the conversion ratio [57, 66]. Sensing the input voltage and changing the conversion ratio to optimize the charge transfer rate helps the converter to recover faster whereas the drop in the input voltage reduces the charge transfer during transient recovery. However, the converters that need to deliver a smaller output current or converters that have better decoupling at the supply input may not cause the input voltage to drop as much and therefore they may not benefit from the conversion ratio manipulation to minimize the input voltage drop during transients. The output voltage or the difference between the input and output voltages can therefore be used to determine the conversion ratio to improve the transient response where the input voltage drop is no longer the limitation [66]. Similar to reconfiguration, this method may also cause a sudden increase in the charge transfer rate which renders the value stored in the integrator incorrect.

This method is implemented with the same converter used in the verification of the model and a verilogA model is used to change the conversion ratio from 1/3 to 1/2 when the input and output voltage difference goes below $V_i - (V_{ref} - 30mV)$. Again, a 100 Ω resistor and additional current sources that step up from 0 to 650 μA and from 0 to 1.3 mA are used as load. The simulation results of this method is given in Fig. 3.16.Changing the configuration yields a faster response as compared to the previous method with 80 ns settling time when the output current step is 1.3 mA. However, when the comparator is triggered with a 650 μA load current step, the settling time increases to 1 μs because the integrator in the control loop holds a value that does not represent the actual charge transfer rate after reconfiguration.

3.4 Addressing the Transient Response Issues

The transient response issues discussed in this chapter are primarily due to the fact that when the operating parameters of an SC converter is changed (when the conversion ratio is changed or when the control parameters are manipulated to speed up the transient recovery), the integrator

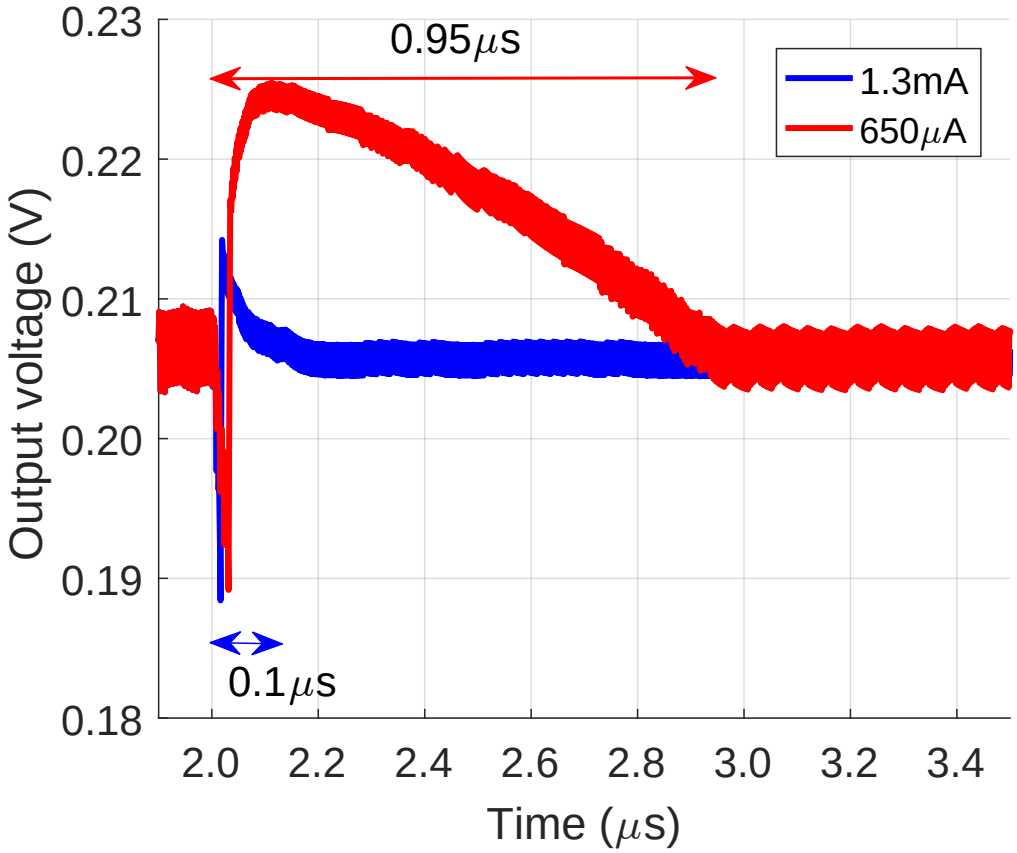


Figure 3.16: Transient response of a 1/3 converter while adaptively reconfiguring to a 1/2 converter to speed up the recovery when the voltage drop is sensed. Two different current pulses of 1.3 mA and 650 μA are used to trigger the reconfiguration. Notice that when triggered by a smaller pulse, the output voltage has a significant spike during the reconfiguration.

in the control loop can no longer follow the actual charge transfer rate to the output (*i.e.* output resistance). Additionally, in most implementations in the literature, the integrator does not have a fast path to settle to a lower value [8, 49, 55, 57, 58, 66] meaning these methods do not improve the response to a decrease in load current or a decrease in reference voltage which is important to maintain low overshoot during reconfiguration or to maximize the power savings in DVS [52]. Integrator in the loop needs to take sufficient number of samples from the output voltage to start following the real charge transfer rate after the reconfiguration or transient response enhancement. Therefore, to effectively improve the transient response performance, the integrator characteristics has to be adjusted adaptively.

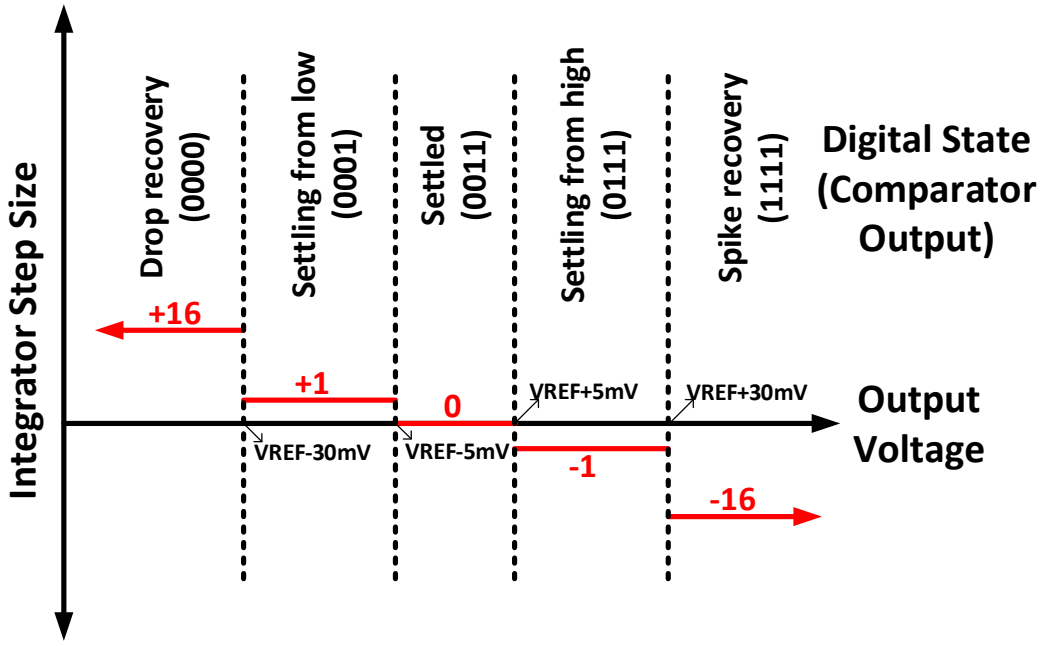


Figure 3.17: Proposed gain modification scheme to prevent overshoots or undershoots. Several states are established based on the difference between the output voltage and the reference voltage and integrator step size is modified accordingly to achieve fast recovery.

A possible technique to increase the settling speed of the integrator is implementing several integrator regions that have different step sizes based on the difference between the output and reference voltages. This proposed adaptive gain-modification, as illustrated in Fig. 3.17, helps the integrator to search for the target value faster than searching with the smallest step. When a voltage larger than 30 mV is sensed in this hypothetical control loop, integrator step size is increased to 16 levels until the output voltage is within 30 mV of the reference voltage. When the output voltage gets closer to the reference voltage, the step size is set to the unit size again to ensure that overshoots do not occur. This method helps integrator to keep up with the actual current requirement at the output rather than setting it to the max value for fast recovery [49]. The proposed adaptive gain-modification can also be used when the output voltage exceeds a certain value because of a decrease in the load current (*i.e.*, idle operation) or because of a decrease in the reference voltage (*i.e.*, DVS operation to save power). This is particularly important since the issues described in this chapter

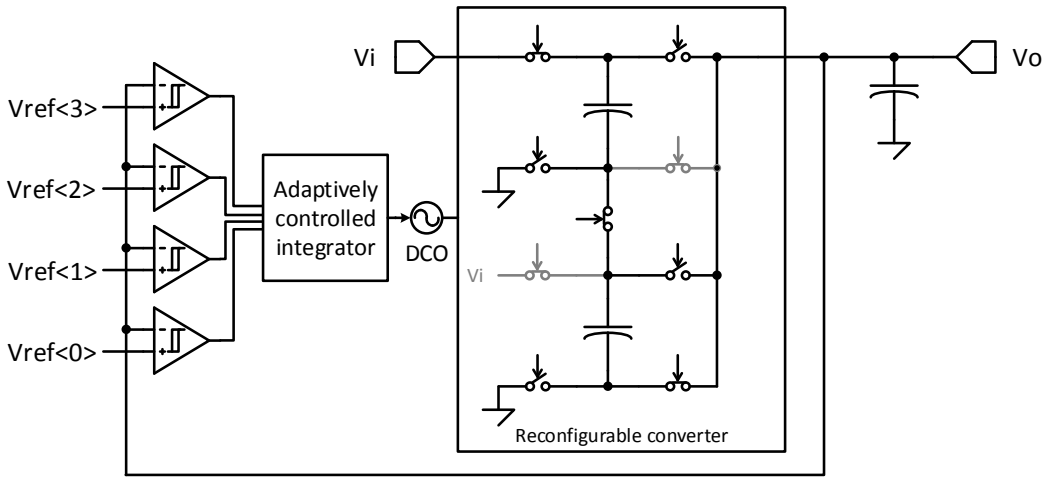


Figure 3.18: Implementation of the proposed method by using 4 comparators. The reference voltages may be given separately or a single voltage reference can be used and levels can be implemented as slightly mismatched comparators.

are mostly the result of the controller's incapability to settle to a lower voltage fast, as apparent in Figs. 3.14, 3.16 and 3.15.

The adaptive gain-modification can be implemented both in analog and digital integrators utilized in the control loops. In a digital integrator, new states can be added where the step size is changed. In an analog integrator, similar to [49], the gain manipulation can be implemented as a modification in the charge pump current during interrupt states. Additional comparators that are triggered at different levels are also required to decide the gain region, as illustrated in Fig. 3.18. For example, the gain configuration given in Fig. 3.14 can be implemented using four comparators. To generate different reference voltage levels, comparators with slightly mismatched input stages or a simple resistor string can be used.

Proposed method of regulation is simulated with the same converter that is used for the previous simulations and the results are given in Fig. 3.19 and Fig. 3.20. In Fig. 3.19, the reference voltage is increased from 200 mV to 260 mV and to 350 mV, respectively. As the converter output current rises suddenly after the reconfiguration, the output voltage starts increasing at a high speed. Unlike the conventional method, however, the proposed method increases the integrator step size to reach the target voltage faster. This does not compromise the stability as the regular operation of

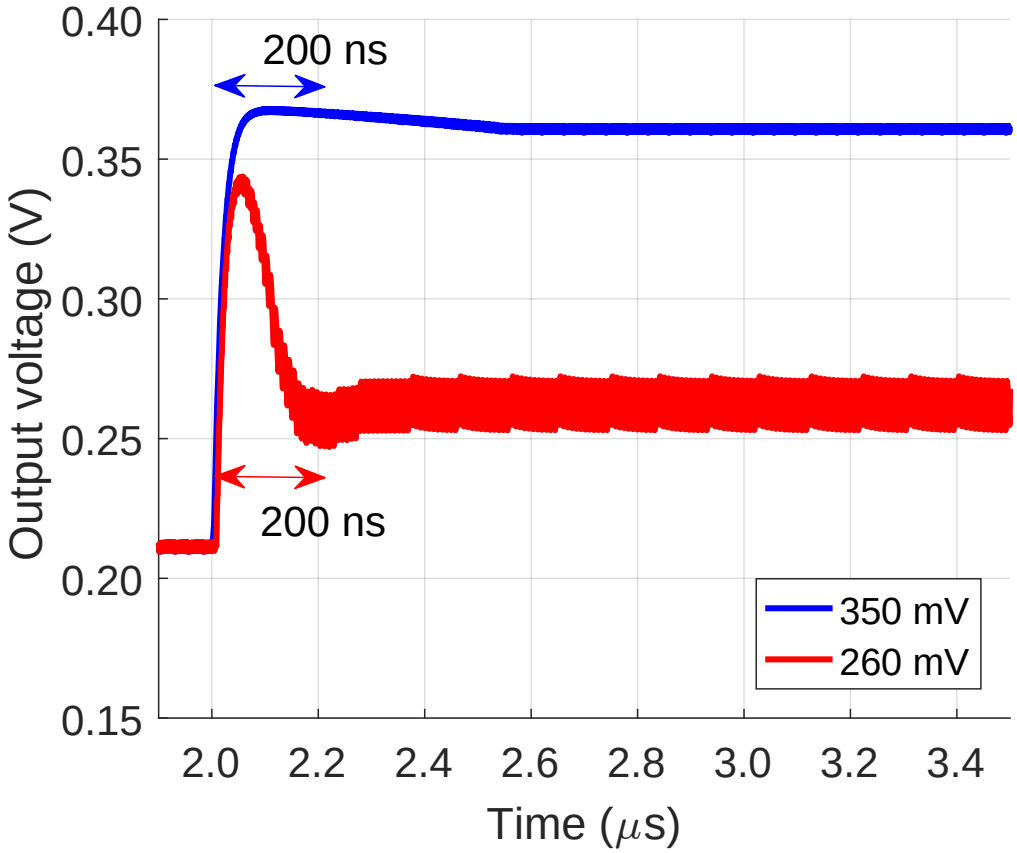


Figure 3.19: Transient response of the proposed control method to a voltage reference change from 210 mV to 350 mV and from 210 mV to 260 mV. Both of these steps cause reconfiguration from 1/3 configuration to 1/2 configuration. Proposed method improves the transient recovery during reconfiguration.

the converter is restored for output voltages closer to the reference voltage. However, too large step sizes must be avoided to prevent the output voltage from entirely skipping the regular operation range in a single cycle. For example, if the step size is set too large, the output voltage may change from a point that is 30 mV lower than reference to 30 mV higher than reference in a single cycle and the control loop will start operating as an on/off converter with high output voltage ripple. As compared to the conventional control method described in Section 3.3.1, the proposed method improves the settling time from 1.15 μs to 200 ns for a sudden increase in the reference voltage from 200 mV to 260 mV. The transient response to load current steps from 0 to 650 μA and 0 to 1.3 mA in parallel with a 100 Ω resistor load for DC current is shown in Fig. 3.20. The load

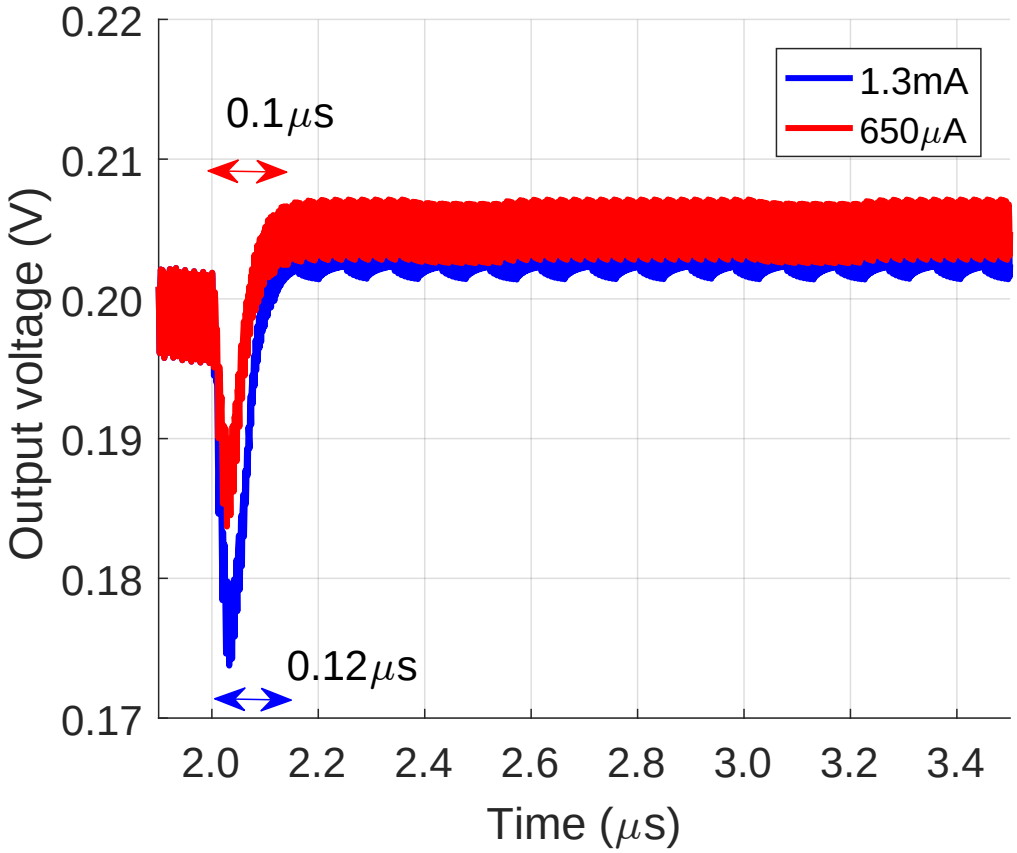


Figure 3.20: Transient response of a 1/3 converter with the proposed control method. Two different current pulses of 1.3 mA and 650 μA are used. Unlike the other enhancement methods, proposed method does not give unexpected spikes when the recovery of a smaller step is improved.

transients are chosen as 650 μA and 1.3 mA, both of which are sufficiently large to trigger the gain manipulation in the control loop. As compared to the other transient enhancement methods, the proposed technique does not increase the settling time unexpectedly when the regular operation is interrupted with a smaller step in the load current or reference voltage.

Similar concepts have been implemented in the literature [8, 66], however, the effects of the control techniques have not been discussed in detail under different load and reference voltage conditions. More importantly, most of the transient enhancement methods do not improve the response to a negative current step (*i.e.*decrease in load current) or a negative reference voltage step

which is important when the converter characteristics change during reconfiguration or response enhancement for DVS systems with wide output voltage range.

3.5 Conclusion

The impacts of reconfiguration on the transient response of a reconfigurable SC converter are discussed in this work. First, a model that extends the analysis of a 1/1 SC converter to different configuration ratios is developed to understand the transient behavior of converters during reconfiguration. The model is used to demonstrate the impact of a sudden increase or decrease in the charge transfer rate during reconfiguration. The change in the charge transfer rate is demonstrated to cause longer transient settling times especially when the reference voltage is set to levels close to the limits of each configuration. This is particularly important for DVS systems which utilize SC DC-DC converters for power management. Control methods that use additional fast loops and reconfiguration are shown to suffer from a similar problem when operated close to their limits or triggered falsely by changing the reference voltage. The recovery from different configurations where the SC converter characteristics are significantly altered is shown to require a fast tracking ability both for a sudden increase or for a sudden decrease in the reference voltage or output current, which is often overlooked. To mitigate these problems, a control loop with adaptive gain-modification is proposed. The gain of the comparator is adjusted depending on the output voltage level sensed by the additional comparators to achieve the fastest settling under any condition. The proposed adaptive gain modification technique improves the transient settling time more than five times from 1.15 μs to 200 ns while also maintaining a uniform response with differently sized load transients.

CHAPTER 4:
IMPLEMENTATION OF AN SC CONVERTER WITH A FAST CONTROL LOOP USING HYBRID CONTROL METHOD IN 28NM FDSOI TECHNOLOGY

4.1 Introduction

Validation of concepts in the field of integrated circuits requires physical implementation of the circuit and measurement results. To prove some of the concepts proposed in this work a test chip is planned in ST 28nm FDSOI process. The objectives of this implementation, design of the test chip and planned testing methodologies will be discussed in this chapter.

While in many cases it is possible to prove the fully integrated concepts with discrete solutions which is easier and with shorter turnaround, most of the techniques examined and introduced in this work such as having 64 phase multiphase converter or transient response improvements that require logic operation are infeasible to implement with discrete elements. Also addressing the effects of full integration will be a part of the future work. Therefore a fully integrated solution will be used in the proof of the concepts introduced in this work.

The ST 28nm FDSOI process is chosen for the test chip because this process offers all the necessary tools for the implementation of SoCs which have significant digital and analog subcircuits and implementation of power management solutions for such systems is the objective of this work and best done in the same process used to design them. The effects of short channel devices on SC voltage converter design is another important topic that requires attention when full integration is concerned and will be investigated using this test chip in the future work. Additionally SC converters are known to benefit from the reduced bottom plate parasitics in FDSOI processes which improves some of the merits of the converter.

Even though the methods described in previous chapters are not mutually exclusive, not all of them can be implemented together without requiring significant changes in the architecture. For example the configuration modification for fast transient recovery described in Chapter 2 prevents the testing of transient response of reconfigurable converters described in Chapter 3. To implement both together an additional option has to be added to the design to enable or disable one of the methods. However adding these options would increase complexity (additional pins and additional logic) which will be avoided as this is the first test chip implemented by the author in this process. So only a subset of methods described in this work will be investigated in this test chip.

In the Section 4.2, the top level considerations for the design are introduced and the architecture is discussed. In the Section 4.3, the implementation of each sub-block (*i.e.* converter core, comparators, oscillator, control logic). In the Section 4.4, the testing methodologies and the expected results are presented and in Section 4.5 conclusions are drawn.

4.2 Architecture of the Implemented Design

The purpose of this design is to create a test platform for fast responding DC-DC converters which exploit advantages of 28nm FDSOI process. The design is also planned to be versatile enough to allow measurements using different external control loops. Fast response will be achieved by a resistance-capacitance modulation hybrid control method with a digital loop that has adaptive gain setting. The second objective which is the exploitation of 28 nm requires trial and error, which is not possible at the time, therefore a good enough power output (20-50 mA) with a mid range efficiency (70-80%) is targeted. The design will be implemented with first working sample being the ultimate goal.

The converter is planned to be a 0.95-2.2 V to 0.4-1.0 V 63 phase integrated switched capacitor DC-DC down converter (in 1/2 configuration) with experimental fast responding adaptive gain digital control loop. The top level diagram is given in Fig 4.1.

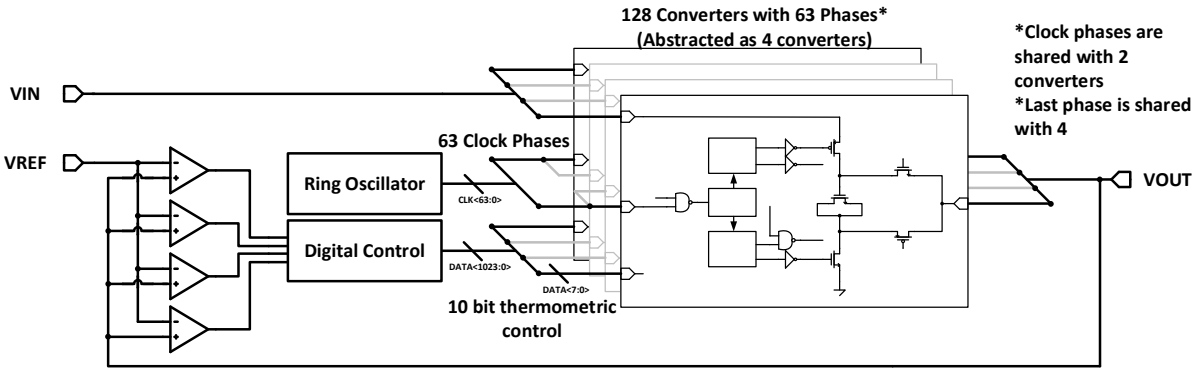


Figure 4.1: Simplified block diagram of the implemented design. The design has 63 phases and each clock phase drives 2 stages except for the 63rd phase.

4.2.1 Hybrid Control Method

In order to implement the described system, it is necessary to have a digital control loop with high granularity. Even though there are methods for implementing fully digital control loop, they usually have overheads which are not suitable for this work. Therefore a hybrid control method combining the benefits of resistance and capacitance modulation is used in this design.

The converter core is divided into 63 phases with each phase operating with a staggered clock to minimize the decoupling requirement and output voltage ripple. In each phase the switch that connects output voltage to the bottom plate of the flying capacitor is again divided into sub switches that are driven with separate drivers. When the appropriate digital data is given, the drivers of the divided switch drive only the portion that corresponds to the input thermometric digital data. This enables resistance modulation to achieve regulation. If all the signals going to a phase is zero, meaning that all sections of the divided switch should be turned off, then the clock going into the phase is shut down connecting the flying capacitor between output and ground. This enables the capacitance modulation in this system. So for small steps the resistance is changed, however, when there is a drastic change at the output phases are completely shut down in an order that would minimize the increase in output voltage ripple. The phases which have the largest phase difference in between them (phases 0 and π for example, full symmetry is not possible for odd number of phases) are chosen as consecutive phases to be turned on or off to minimize the increase in output voltage ripple. The process is repeated for each phase until there are no phases turned

on or off meaning that the output can not be regulated for this load, or if the converter is turned off entirely.

4.2.2 Adaptive Gain Selection

The transient response of the converter is enhanced with an adaptive gain digital control loop. The loop is made up of 4 comparators and a digital integrator with several different operating states as shown in 4.1. 4 comparators in the loop have mismatched input stages (reasoning for this will be explained later) and the mismatch values are chosen to ensure that the lowest comparator trips roughly around REF - 30 mV, the second one REF - 5 mV, the third one REF + 5mV and the fourth one REF + 30 mV. The 4 bit result from the comparison with rough values around the reference voltage creates 5 different gain regions for the integrator to operate. The first region is the region when the output voltage is more than 30 mV lower compared to the reference voltage, meaning that the gain can be increased. Based on this information, integrator value is increased a predetermined number in every clock cycle the output remains in the same state, instead of being increased a single step every cycle. The second region is the region when the output voltage is within REF - 30 mV and REF - 5 mV range in which a high gain may cause integrator output to overshoot or undershoot, therefore the integrator is set to step up one at a time. The third region is where the output voltage is between REF - 5 mV and REF + 5 mV. This region is considered to be the region where the loop is settled and to prevent any unnecessary ripple at the output integrator retains its value. The fourth and fifth regions are the complementaries of the first and second regions except in fourth and fifth regions the integrator value goes down as the output is higher than the reference voltage level. This approach yields a faster result compared to the conventional single gain setting without causing overshoot or instability. The proposed implementation is summarized in Fig. 4.2 More importantly this approach also improves the response to a negative load current or reference voltage step which is very important for dynamic voltage scaling.

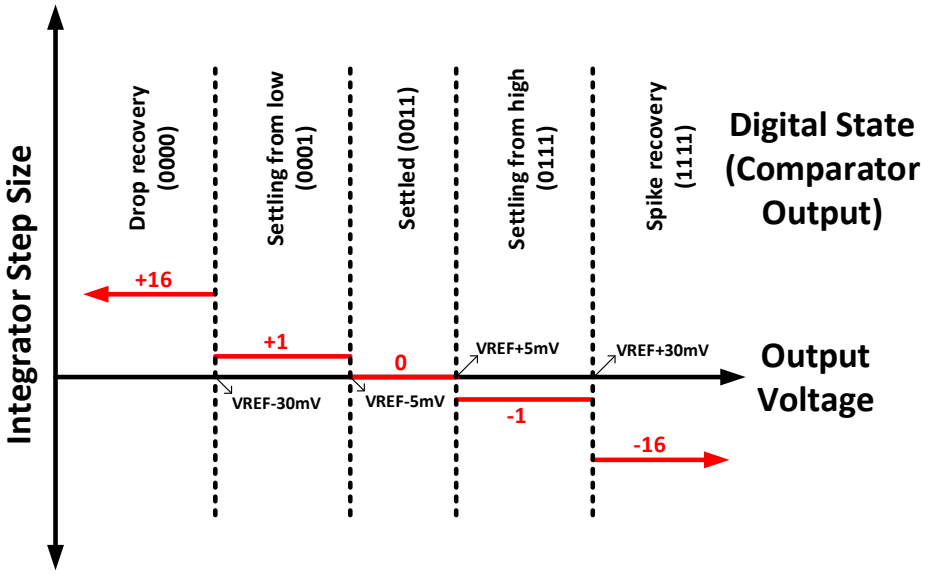


Figure 4.2: Gain or the step size of the integrator is modified according to the difference between the output voltage and the reference voltage to help fast recovery.

4.3 Implementation of Sub Circuits

The system is implemented as modular as possible in order to simplify the design and testing. Modular design also helps with the implementation of backup options which is important since the first pass success is the goal in this design.

Each subsystem will be investigated in this section.

4.3.1 Switched Capacitor Core

The switched capacitor core represents the part where the switches and flying capacitors are implemented. SC core was originally planned to be a multiphase reconfigurable SC converter, however because of time limitations and uncertainty with some of the process safe operating area checks the choice is deemed risky. As a result only the 1/2 converter is implemented in the design.

The implementation of the SC core is given in Fig. 4.3. Transistors P1, N1, N2, P2 and Nfly form the basic 1/2 converter in this implementation. N1 and N2 are chosen as NFETs since this way these transistors can be driven with the same phase shifted signals, simplifying the driver and

clock generator implementation. P1 and P2 are again chosen as PFETs to simplify the driver and clock generation. The simple implementation for phase generation and level shifting is important in this design because the reliability and first pass success are the main goals even though there are implementations which may provide better efficiency. For the flying capacitor which is implemented as NFET named Nfly, the choice is made because NFETs in this process can be realized as deep-N-well transistors. This mainly helps with two important operational characteristics: i) safe operation with high voltages, ii) increased efficiency through floating deep-N-well connection. As long as the junction diodes remain within 6 V limit and as long as gate oxide limits are not exceeded, the voltage on gate and source-drain nodes of this transistor can be made larger than the regular VDD levels. Operating a PFET in this configuration is not always favorable as the N-well is usually tied to a constant voltage. More importantly, since the deep-N-well can be independently biased NFET flying capacitor can achieve lower bottom plate parasitic capacitance which significantly increases the efficiency as explained in [49]. The deep-N-well connection in this implementation is made through a resistor which effectively leaves the well connection floating for any transient signal during switching. Leaving the well connection floating during transients mean that the total capacitance seen from the drain-source node of the transistor is reduced to the series equivalent of bulk-deep-N-well capacitance and deep-N-well-substrate capacitance.

Inside the SC core, the PFET P2 is divided into 8 equal pieces and driven separately. A digital signal named data<7:0> which is generated by the control loop determines how many pieces of the P2 PFET needs to operate at a given output power. The ones that are not needed are simply turned off by using a NAND gate and set to a constant high voltage. Scaling the size of P2 modulates the resistance which again changes the charge transfer rate to the output. If all the parts of P2 are turned off, the clock given to this core is gated using a NAND gate. Turning off the clock saves the power lost in driving other transistors and non-overlap generator and enables a version of phase or capacitance modulation.

The outputs of the non-overlap generator is given to level shifters which shift the voltages to different voltage ranges which are VIN-VOUT and VOUT-AGND. Since all the transistors in the core circuit are thin oxide transistors this level shifting makes sure that none go beyond their

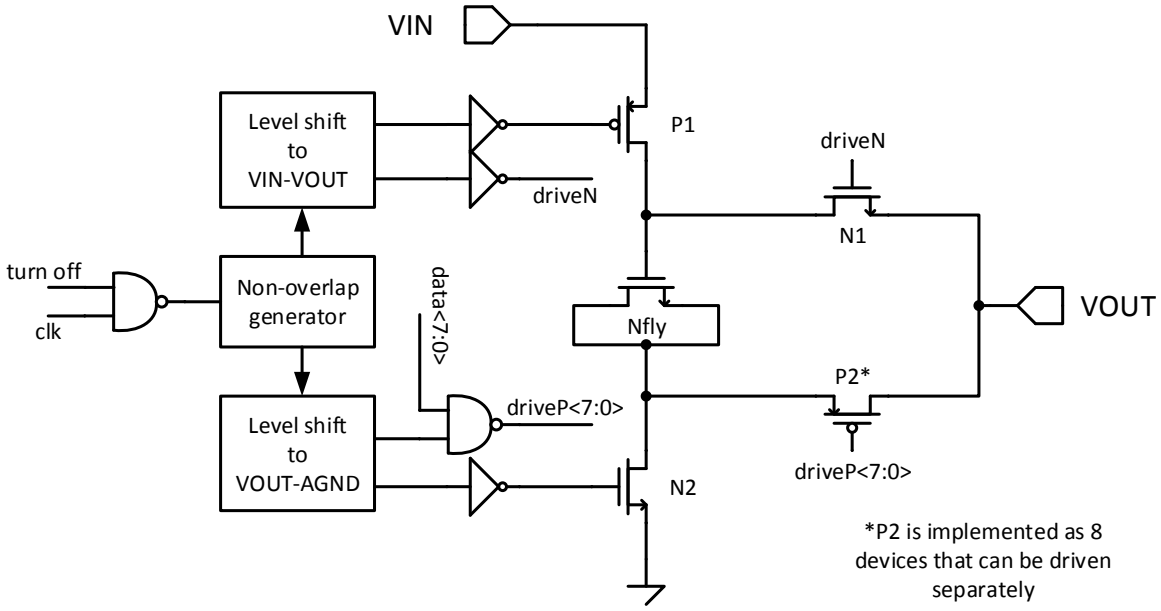


Figure 4.3: Switched capacitor core includes a divided switch which has parts that can be driven separately to allow charge control to the output.

safe operating region. However this also causes a few startup issues when the output voltage is low and VOUT-AGND is not high enough to switch N2 and P2 which will be discussed in testing. To simplify the clock distribution and level shifting, all the clock signals are in VIN-AGND domain. Having high voltages available enables the use of level shifters that are only positive feedback circuits without dedicated capacitors to create voltage drop. This implementation requires the use of thick oxide devices in the clock distribution network which complicates the layout to a certain degree since there is a separate rule dictating the distance between the thin oxide region from thick oxide region. However having more reliable level shifters are chosen as a goal and therefore high voltage clocking network is used.

The layout of the SC core is given in Fig. 4.4. The sections on the right are the pieces of the floating capacitor. The capacitor is implemented in segments in order to reduce the series resistance to gate and source-drain nodes. However because of the latch up prevention rules and oxide rules the capacitor has to be separated from the rest of the devices with wide guard rings with width of at least 5 um and the same limitation applies to every location a thick oxide and thin oxide well

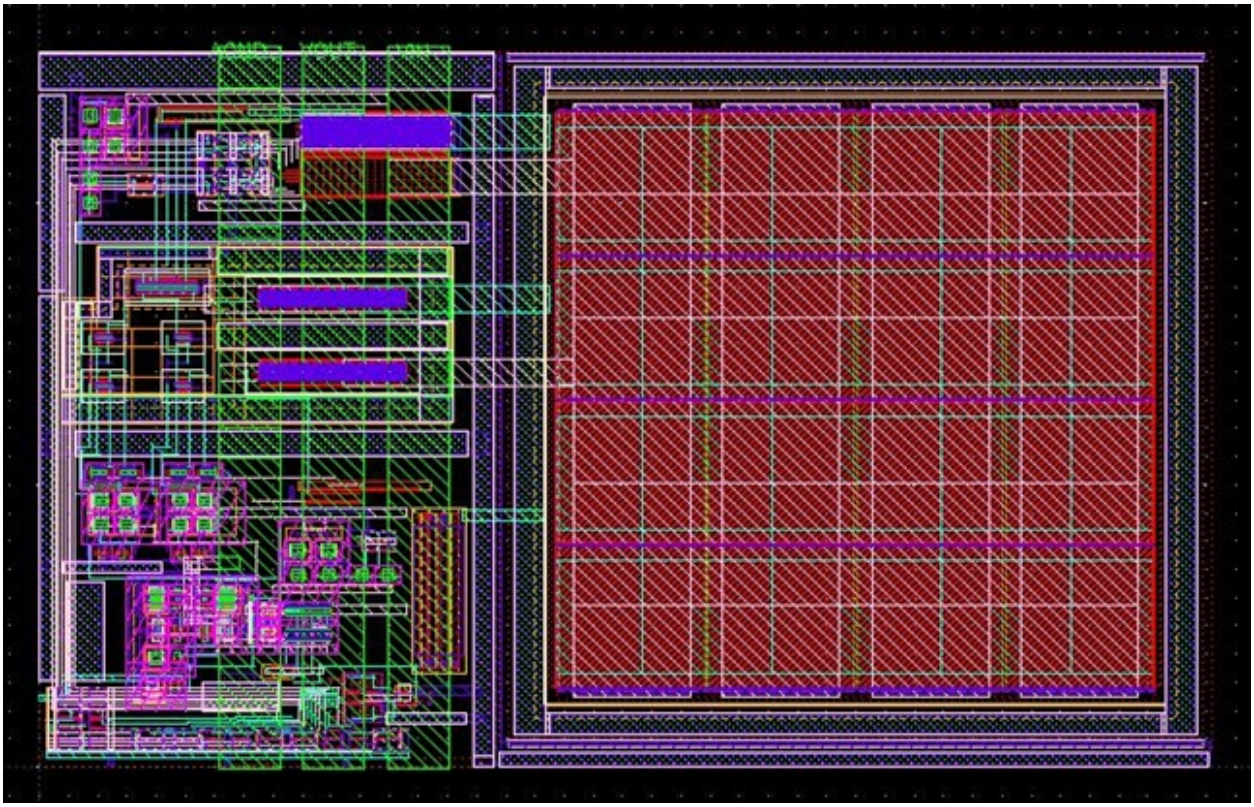


Figure 4.4: Layout of the switched capacitor core circuit

with different voltages are placed. As seen from the black portions on the switch and level shifter side (left part) some area is occupied by guard rings to satisfy this rule. The three green strips make up the metal 4 layer which allows the connection of AGND (analog ground), VOUT and VIN to higher metal layers are placed as strips to form a single line when the cores are put together.

64 SC cores are used in the final design, meaning 1024 different levels are available for control and 64 clock inputs for multiphase operation. A single SC core operates nominally at 200 MHz with 75% efficiency while delivering 720uW at 0.72V from 1.8V supply. Expected operating input/output voltage range is 0.7-1.1V input and 1.6-2.5V output.

4.3.2 Comparators

4 comparators are used to sense the voltage level at the output. The comparator architecture is chosen as double-tail latch-type comparators for speed and low kickback noise. The implementation of a single comparator is given in Fig. 4.5. The M1 and M2 PFETs form the input differential

pair, M3 and M4 form the active load. When the CLKB signal is high, the M3 and M4 transistors pull their drains to ground effectively resetting the amplifier and latch stages of the comparator. It is important to note that during this stage back to back connected inverters in the latch part is also reset. To prevent the back to back converters to conduct current in this phase M10 is added to turn the current to the latch side off and reduce the power consumption that would otherwise be caused by the back to back connected inverters being forced to the same state. When the CLKB signal goes low, M3-M4 transistors are turned off forming an active load and M9 transistor operates as a current source. Depending on the difference between Vin+ and Vin-, the drains of M3 and M4 both get charged at different rates compared to each other. For example if the Vin+ is higher than the Vin- the drain of M3 charges up much slower than M4. The voltage difference at the drain of M3 and M4 is further amplified by M5 and M8 which act as an intermediate gain stage. As soon as the drain voltages of M3 and M4 reach a level that turn on M5 or M8, the positive feedback in the back to back connected inverters start generating a response based on the input conditions. This type of comparators i) can respond very fast without a transition state since the outputs are reset ii) cause less kickback noise than single branch dynamic comparators since the first stage acts like a buffer amplifier.

In the implementation of the proposed method, 4 of these comparators are needed to determine the output voltage. The comparators also need different voltage references to be able to determine how far the output is from the reference voltage level. A resistor string can be used to generate the separate voltage levels required based on the reference voltage given to the regulator. However, this requires reference driver to drive a large current to the resistor string to overcome the noise from the comparators. Moreover since the voltage reference will be divided in the resistor string implementation, the feedback signal from the voltage output of the SC converter has to be manipulated as well. In order to mitigate these effects, instead of generating voltage levels, the input stages of each comparator is manipulated. Each comparator input stage is divided into 50 fingers and the number on each side is manipulated to create an offset around the reference voltage. For example the comparator that compares the output voltage with VREF+5mV has 49-51 finger distribution in its M1 and M2 transistors. Similarly the comparator that compares the output

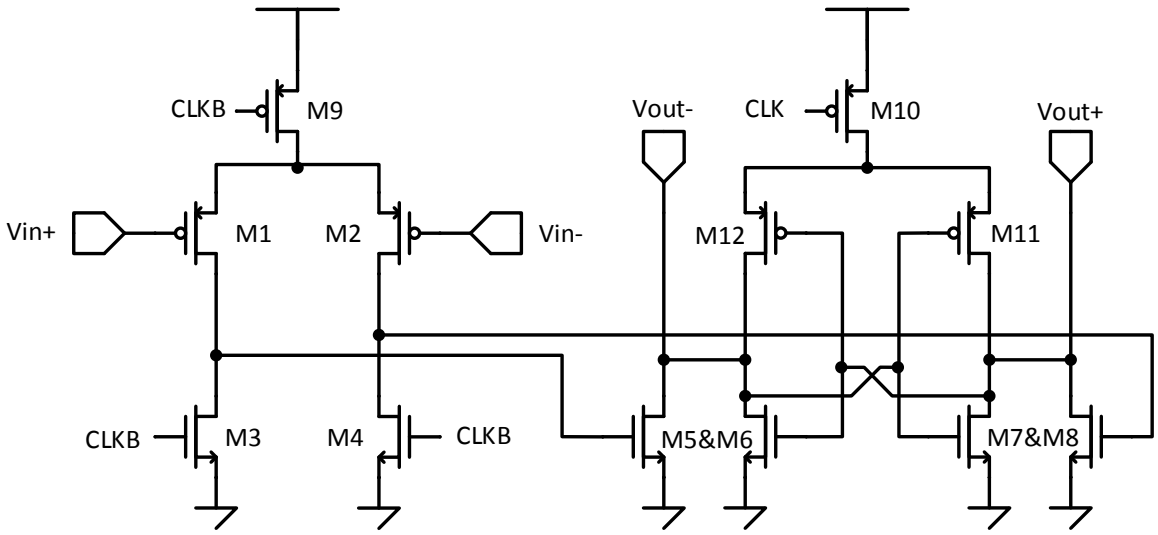


Figure 4.5: A dynamic comparator is used in this design to reduce DC current. The double tail comparator is chosen to reduce the kickback noise.

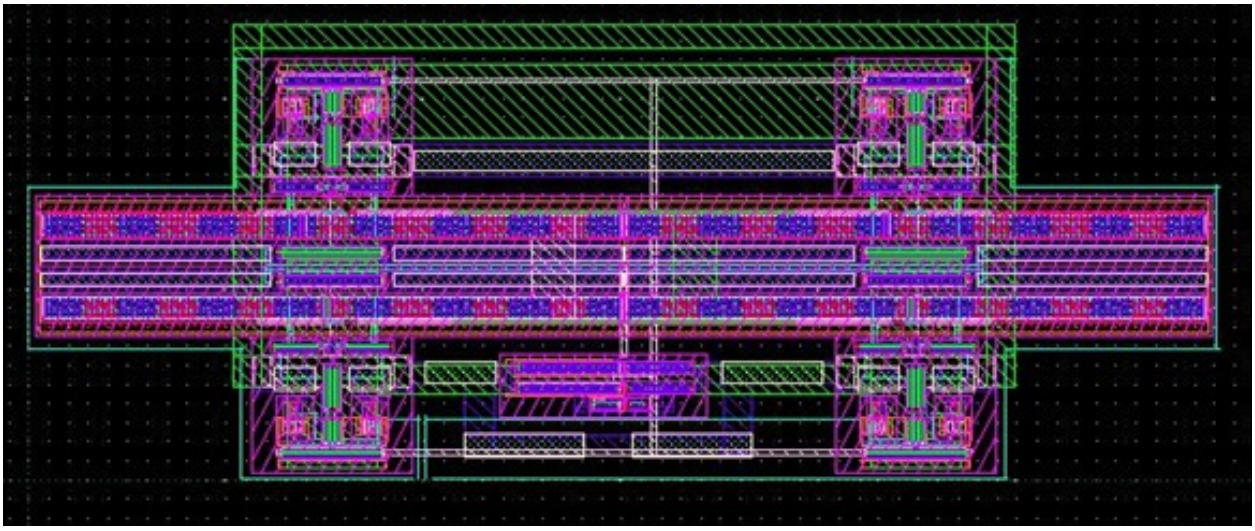


Figure 4.6: Layout of the 4 comparators

voltage with VREF+30mV has 41-59 finger distribution. This implementation is very susceptible to process variations however it eliminates the need for a reference driver and does not load the SC converter's output with extra resistance. In the case the comparators fail because of offset an option to use external comparators is implemented in the logic and pad ring.

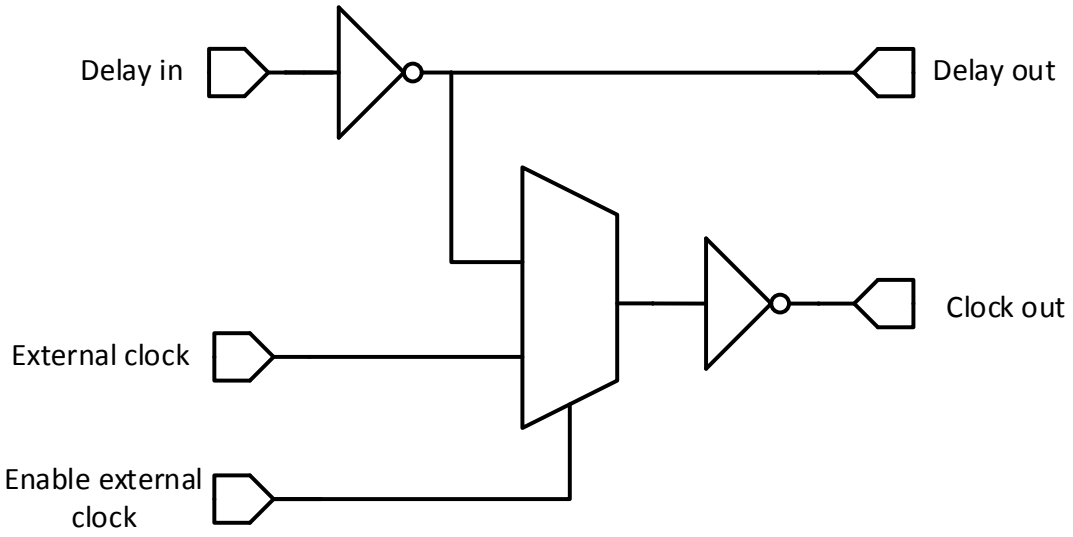


Figure 4.7: The delay cell of the oscillator has buffers to maintain uniform phase distribution. External clock option is implemented in each cell and if enabled all the phases are given the same clock.

The layout of the 4 comparators is given in Fig. 4.6. The main consideration in this layout is the offset of the input transistors and signal propagation delays. To achieve the lowest offset for the comparators all 4 input stages are put together as close as possible in the central strip. The propagation delay from clock signals to each comparator causes the samples taken from the output voltage to be different which affects the accuracy. Therefore all the clock signals are routed as symmetrically as possible.

This comparator is capable of operating at frequencies up to 300 MHz with approximately 1 mV resolution. The standard deviation for offset for the input stage transistors used is 3 mV, therefore the comparators may fail to determine the output voltage region correctly. An external comparator option is implemented as a backup alternative.

4.3.3 Oscillator

An internal oscillator is needed to generate the multiphase clock signals required in the design because delivering many clock phases into the chip is not always feasible because of limitations

regarding number of pads available for a design. The oscillator in this design is implemented as a 63 piece ring oscillator. A single cell of this oscillator is given in Fig. 4.7. Delay in is the input from the previous stage and delay out is the output given to the next stage. To minimize the loading effects and uneven clock distribution a buffer is used at the clock output that will be given to the rest of the circuit. Before this buffer a multiplexer is used to choose between the external clock and the internal oscillator clock. 63 of these stages form a loop and create a ring oscillator that nominally oscillates at 280MHz but this value is expected to drop after production and get closer to the nominal operating frequency of the SC core.

The layout of the oscillator is given in Fig. 4.8. The oscillator is implemented as a line that curls three times and connects to the first stage. The possibility of distributing the stages of the oscillator into each converter core was discussed however this would require a perfectly symmetric layout to prevent uneven distribution of clock phases. Instead, the oscillator is implemented as compact as possible and the clock distribution network is designed to minimize the propagation delay difference between stages driven by different clocks. Additionally turn on/off patterns of the converters are chosen to minimize the effects of the difference in clock propagation delays.

4.3.4 Control Logic

The control logic is entirely written in verilog, synthesized, placed and routed using Cadence tools. Main purpose of this circuit is implementing the digital integrator which tracks the output voltage level and adjusts the output resistance of the converter accordingly. Additionally, since the digital circuits are more reliable many backup options are implemented in this section.

The main control loop implements the behavior described in Fig. 4.2 by increasing/decreasing the integrator value or keeping it constant. The 10-bit integrator value is then turned into thermometric coded digital signal and given to the converter circuit which in turn arranges the switching pattern of its switches. The entire verilog code is given in the Appendix A.

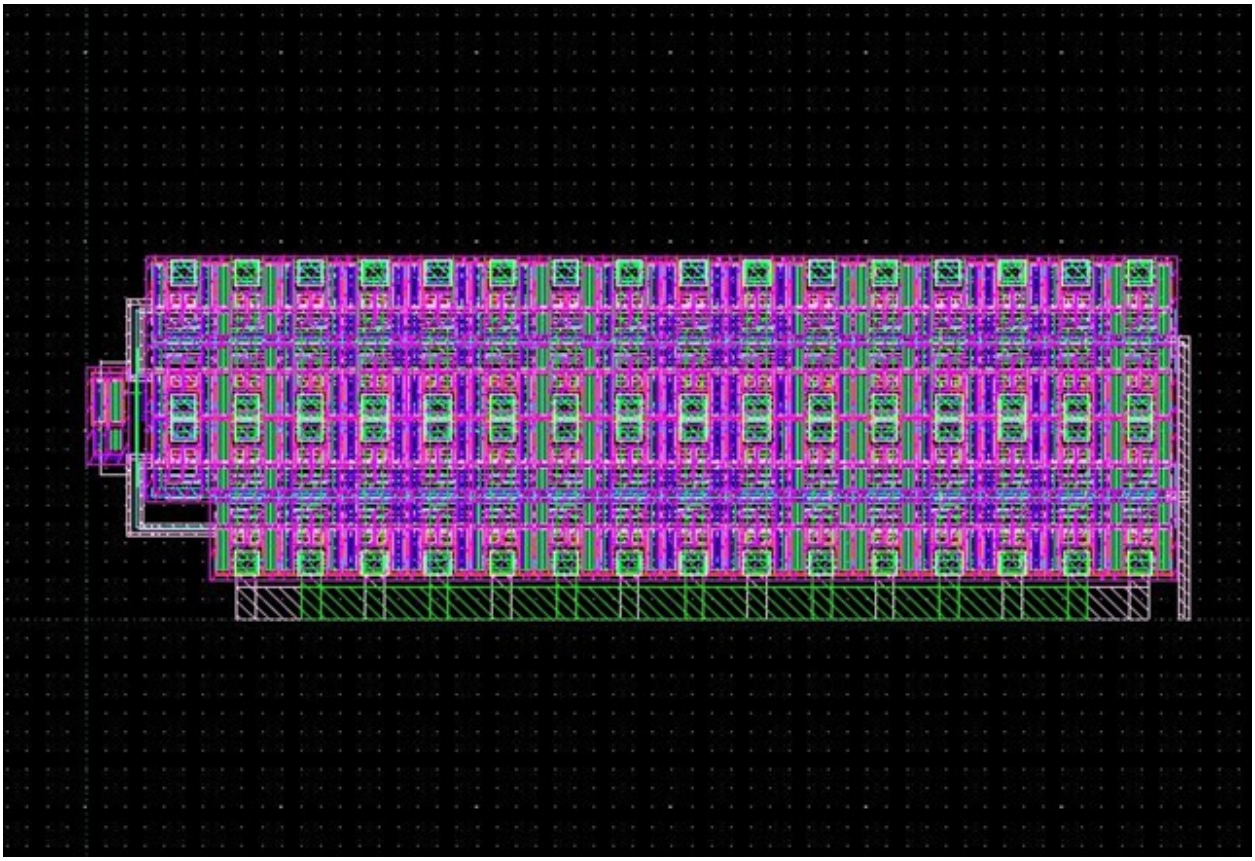


Figure 4.8: Layout of the ring oscillator

4.3.5 Top Level

The complete circuit includes 128 SC cores, driven by 63 phase clock signals operating at 200 MHz (expected), and is controlled by 10 bit thermometric coded signal that manipulates the number of active SC cores and the number of switch pieces active in each SC core. Since there is 63 clock phases and 128 SC cores, every 2 cores get the same clock and the 63rd phase is given to 4 SC cores. As the last phase is only activated when the converter is operating at full capacity, it is not expected to cause a significant increase in the output voltage ripple.

The converter, as explained before, uses a hybrid resistance-capacitance loop in which entire SC cores are shut down. This causes uneven distribution of phases since some of the clock signals going into some SC cores have no effect at the output when the SC core is shut down. To mitigate the increase in the output voltage ripple two separate measures are taken: i) the clock phases that

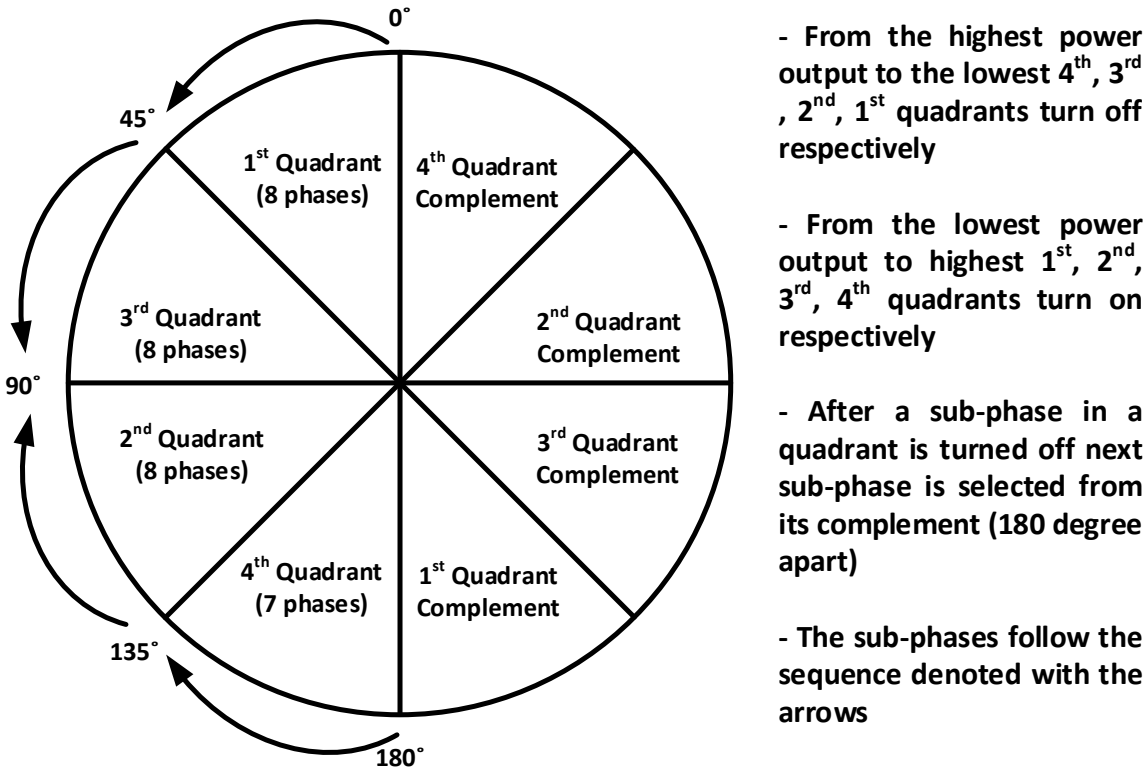


Figure 4.9: Sequence used to turn SC cores on/off is chosen to minimize the output voltage ripple by distributing the clock phases as evenly as possible.

will be turned on or off are selected to maintain symmetry as much as possible, ii) the SC cores that are turned off are connected to the output as extra decoupling capacitors. The organization of phase turn on/off sequence is given in Fig. 4.9. So at the highest power output all the phases are on, and when the output power starts dropping first the pieces of the 4th quadrant from the end to the beginning are turned off and then it is followed by 3rd, 2nd and 1st quadrants. Whenever a piece from a quadrant is turned off the next phase that will be turned off is chosen in its complement (180 degrees phase shift) to minimize the timing difference between each phase. Although a more efficient phase distribution is possible, this scheme allows simple implementation and helps eliminate the clock skew effects when combined with the layout methods used.

Several options are implemented in this design to add redundancy and allow measurements for comparison with regular operation. These options and the pin configuration will be explained in Section 4.4.1.

The top level layout of the circuit is given in Fig. 4.10. The total die area is 1mm by 1mm. 81.598um by 416.524um is the size of each quadrant and there are four quadrants. Each piece of these quadrants are actually a single SC core which is 40.169um by 25.274um and each quadrant is made up of 32 of these cores. 12.003um by 35.785um is the rough total area of the comparator and ring oscillators, however this area is mostly routing and the active area is significantly smaller. 70.809um by 69.600um is used for the digital control and options implemented in digital. The chip will be placed in a QFN64 package and the pin diagram is given in Fig. 4.11. The connection between the die and the package is given in Fig. 4.12.

4.4 Testing and Expected Results

The basic test setup is given in Fig. 4.13. Mainly 4 types of tests are planned:

- DC characterization
- Transient response characterization
- Backup alternatives if one or more sub circuits are failing
- Alternative measurements for different purposes

The test setup to be used for the first three type of tests is given in Fig 4.13. The options and registers are planned to be controlled by an FPGA. This FPGA will also control the state of the resistor bank (disconnected, heavy load, low load) that is to be implemented on the board level for transient response measurements. The external clock and reference voltages are planned to be given using an arbitrary waveform generator. The accuracy of the arbitrary waveform generator is enough for the reference value and the properties of the external clock such as duty cycle can be set. Power to the pin VIN will be delivered using a source measure unit which also has a channel that can also be used as a load for full DC characterization, however, this unit is incapable of generating

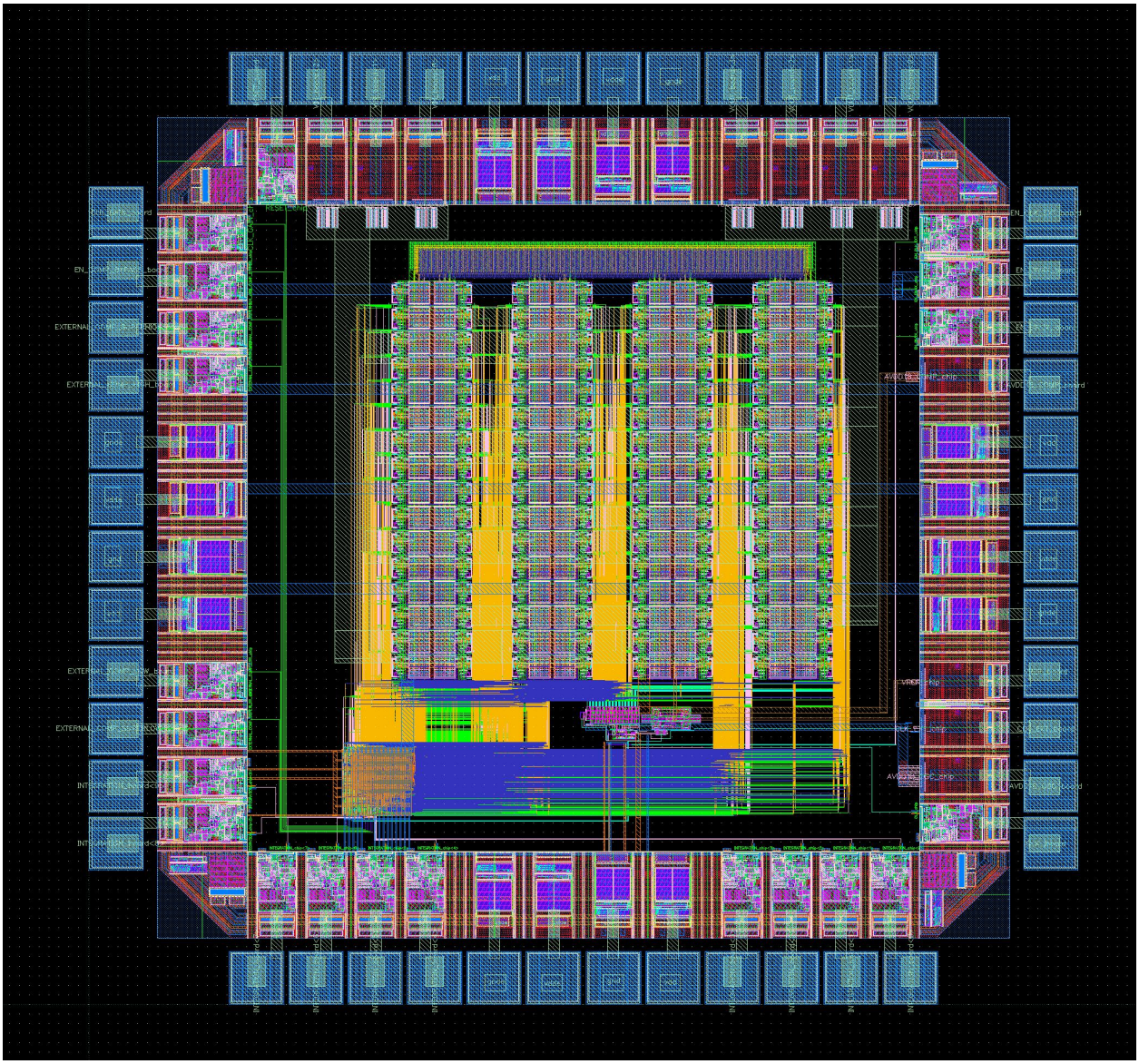


Figure 4.10: Top level layout of the design

the transients with the desired rise and fall times. Other power domains will be supplied by a power supply and the current will be sensed using multimeters. For the transient waveforms, a fast mixed signal oscilloscope will be used. This mixed signal oscilloscope can also be used to acquire (but not set) the INTEGRATION<9:0>values.

First the options and required configuration will be explained, then each of the tests will be explained.

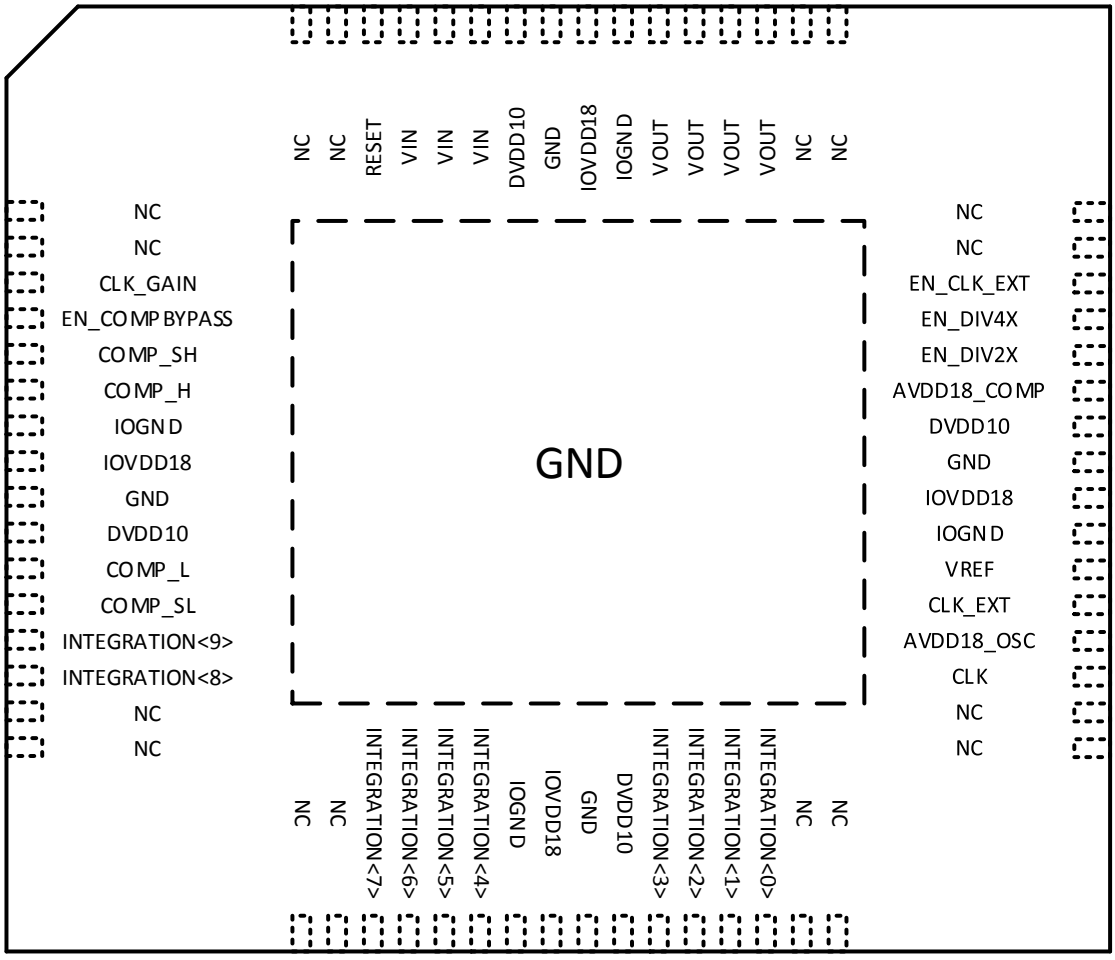


Figure 4.11: Package and pin configuration of the design

4.4.1 Options, Pins and Configuration

Wide variety of options are implemented to increase the reliability in case some of the internal circuitry do not work. These options and the explanations of all the pins are given in Table 4.1.

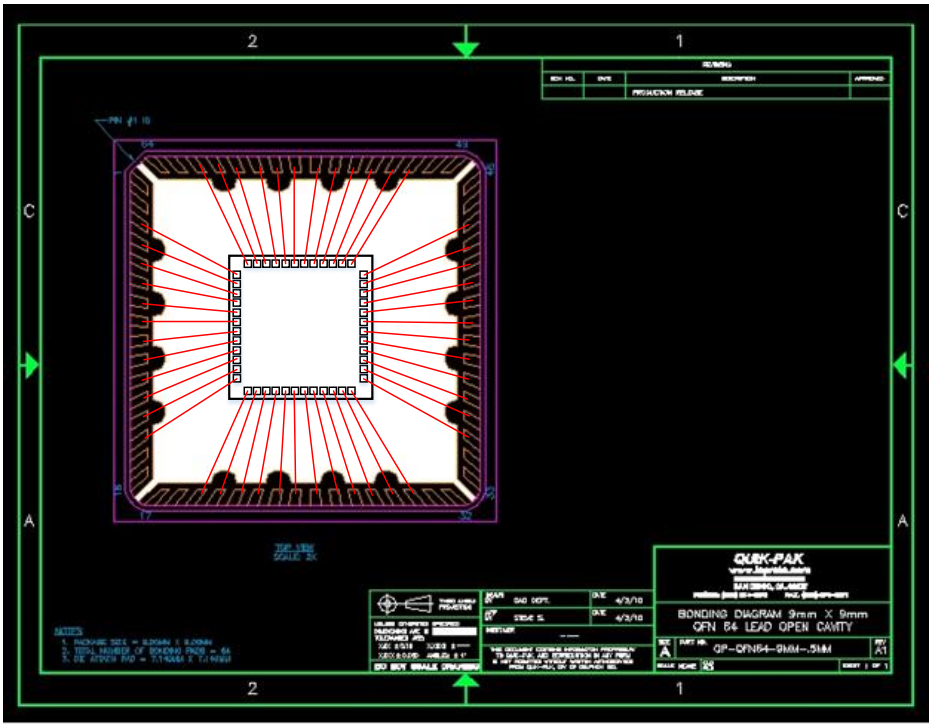


Figure 4.12: Bondwire diagram

Table 4.1: Pins and Descriptions

NAME	I/O	DESCRIPTION
VIN	I	The input voltage pins, 3 of these are required to maintain safe operation.
VOUT	O	The output voltage pins, 4 of these are required to maintain safe operation.
DVDD10	I	1.0V digital power supply, supplies power to the digital circuit and some level shifters.
IOVDD18	I	1.8V supply for IO ring, it is used by the IO pads, ESD structure and some buffers.

Table 4.1: (Continued)

AVDD18_COMP	I	1.8V supply for comparators, no other circuit uses this supply.
AVDD18_OSC	I	1.8V supply for the oscillator, no other circuit uses this supply.
IOGND	I	Ground for IO pads, shorted to GND.
GND	I	Ground.
RESET	I	Reset signal, resets the digital state to a known value given in verilog code.
EN_CLK _EXT	I	Enables the external clock option if 1.8V. All clock signals are connected to single source from CLK_EXT. No multi phase operation is possible.
EN_DIV4X	I	Divides the clock signal of the control loop and comparators by 4 if 1.8V. This is added in case controller becomes unstable. Never give 1.8V to both EN_DIV4X and EN_DIV2X together.
EN_DIV2X	I	Divides the clock signal of the control loop and comparators by 2 if 1.8V. Never give 1.8V to both EN_DIV4X and EN_DIV2X together.
EN_COMPBYPASS	I	Overrides the internal comparators if 1.8V. If enabled, the comparator data is taken from COMP_SH, COMP_H, COMP_L and COMP_SL pins.

Table 4.1: (Continued)

CLK_EXT	I	External clock signal that is used when EN_CLK_EXT is enabled.
COMP_SL	I	External comparator signal for extreme drop recovery (VREF- 30mV).
COMP_L	I	External comparator signal for settling from low
COMP_H	I	External comparator signal for settling from high
COMP_SH	I	External comparator signal for extreme spike recovery (VREF + 30mV)
CLK_GAIN	I	Clock signal that drives a 5 bit counter in the digital portion that determines the step size when extreme drop or spike recovery is engaged. Reset value is 1.
INTEGRATION<9:0 >	O	Data in the integrator for debugging purposes.
CLK	O	Replica of the clock signal for debugging purposes and for oscillator trig. Replicates the external clock if enabled.
VREF	I	External reference voltage that drives the control circuit.

Most of these options are implemented in the digital portion of the circuit to avoid any errors in the design. Some options like EN_DIV4X and EN_DIV2X are mutually exclusive while most can work combined with others.

4.4.2 Test Scenarios

Several test scenarios are needed to fully characterize the converter. In this section first the checks needed to verify the operation of the chip are described and then the test scenarios are explained. In these test scenarios the setup given in Fig 4.13 can be used. The specific differences for each scenario will be explained in their respective section.

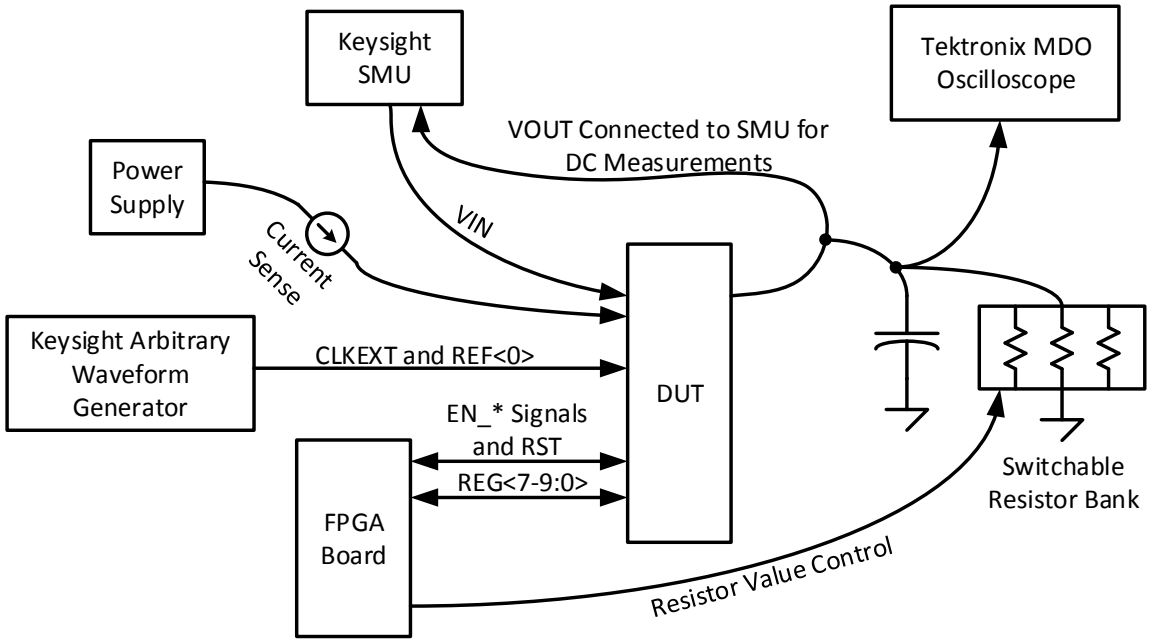


Figure 4.13: Test setup includes several different configurations for DC and transient measurements.

4.4.2.1 Checks

Verification of the minimal operation of the circuit is the first priority in the measurements.

First the operation with zero external input needs to be checked. To do this following steps can be followed:

- Give nominal voltages to all supplies
- Set VIN 1.8V
- Include a pullup resistor connected between VIN and VOUT to startup the circuit
- Disable external clock option
- Disable external comparator option
- Enable clock division by 4

- Disable clock division by 2
- Do not change the gain of the integrator, in other words do not apply any signal to CLK_GAIN
- Give a reasonable voltage (0.7V) to VREF

Under these conditions the circuit should be able to operate nominally. It is important to note that pullup resistor should be switched off after initial settling. The pullup resistor is required for verification because in some corners the lowest operating voltage of VOUT-GND level shifters may cause issues when the output voltage is very low and they may not be able to startup without external pullup. The oscillator operation can be verified by looking at the CLK output which replicates the oscillator signal. However, if the divided frequency of the oscillator is above 100 MHz the IO pad may become the limitation, therefore use division by 4 to verify the operation. The digital loop operation can be verified by looking at the INTEGRATION output, this value should track the load current demand. To precisely investigate the operation of the digital loop, the comparator bypass option can be enabled and appropriate inputs can be given to look at their effects on the INTEGRATION output. Comparator operation can also be verified by looking at the INTEGRATION output, however in order to verify this the gain of the integrator has to be changed because otherwise the steps for the upper and lower comparators will be the same. To change the integrator step size for drop and spike recovery clock the CLK_GAIN signal a few times.

4.4.2.2 Efficiency and DC Performance

The efficiency and the DC performance of the converter can be entirely characterized using a single SMU (Source Measure Unit) as these are capable of providing an accurate input voltage and an accurate output load. The DC characterization with SMU will be a single sweep in nominal case with target measurements being: i) input/output voltage range ii) output current range iii) power efficiency. The reference voltage value is also planned to be swept and one channel of the arbitrary waveform generator will be used for this purpose.

In this measurement the step size of the integrator and the clock division does not matter because as long as the loop settles the results will be the same. Since all the subcircuits get their own supply pin, contributions to the losses can be analyzed separately.

4.4.2.3 Transient Response

The transient response of the converter will be measured in two ways: i) by changing the reference voltage (closer imitation of a dynamic voltage scaling scenario) ii) by changing the load resistance. First option is planned to be implemented using the arbitrary waveform generator. By changing the reference voltage up or down the response of the converter in a dynamic voltage scaling system can be characterized. Second option will be implemented as a resistor bank that is realized at board level. The resistor bank and switches will be controlled using an FPGA, however the exact implementation has not been addressed yet and power switches may be needed. These resistors will cause fast changes in the load current demand. Effects of both of these changes will be recorded using the oscilloscope which is planned to be triggered with the replicated clock from CLK output or using a signal from the FPGA.

4.4.2.4 Backup Plans

All three subsystems (comparators, integrator, oscillator) can be replaced as long as the converter core is working.

If the oscillator is failing, EN_CLK_EXT setting can be used to input an external clock that is generated by the arbitrary waveform generator. In this case the multiphase operation is omitted. DC characteristics are not affected, however the ripple performance and transient response are expected to be worse.

If the integrator is failing, the data in the integrator can be set to a known value using RESET, however any change will probably cause integrator to fail again therefore making this unusable for transient characteristics. In this case the transient measurements cannot be completed, DC characteristics of the core are unaffected but harder to measure.

If the comparators are failing, EN_COMPBYPASS setting can be used to set the comparator values externally. None of the measurements are affected in this case, however an external comparator setup is needed and without using clock division the clock signals (if necessary) will be harder to deliver to the comparators.

4.4.2.5 Measurements for Comparison

Several measurements are planned to provide comparison with other methods explained in literature. For example the CLK_GAIN option can be used to mimic the behavior of a conventional control loop, and the effects of changing the integrator step size adaptively can be precisely pointed out. Alternatively, effects of multiphase operation can be investigated by using internal clock and then comparing it to the external clock operation for the same output load. Unfortunately converter reshuffling is not implemented in this design.

4.5 Conclusion

A SC DC-DC converter in 28nm FDSOI process is designed and submitted for fabrication. The design focuses on being simple and reliable to start a test platform for future implementations. The expected results are 75% efficiency from 1.8V supply while delivering 92 mW while occupying 240um by 420um area. The proposed method is expected to improve the transient response time to increasing or decreasing reference voltage or increasing or decreasing output current. Implementation and planned test structure is explained, however the fabrication has not been completed so no measurement results are given.

In the future work, this converter will be extended to operate as a reconfigurable converter with more than one ratio and will be modified to support some of the hardware security measures described in this work.

CHAPTER 5:

CONCLUSIONS AND FUTURE WORK

This work provides an understanding of how SC voltage converters work and further focuses on improving several aspects of SC voltage converters. A fully integrated solution is chosen as the ultimate goal since the integration reduces the PCB footprint, increases reliability and allows optimization of critical voltage converter characteristics such as transient response or voltage drop while maintaining similar performance in other characteristics compared to conventional solutions. The SC voltage converter is chosen for the fully integrated approach because of its simple implementation and compatibility with modern IC processes as pointed out in detail in Chapter 1. Improving the characteristics of a voltage converter that benefit the most from integration makes up the motivation for this work as explained in Chapter 1. The characteristics that are the focus of this work can be listed as:

- Improvement on power efficiency and density of SC converters
- Improvement on transient response to load fluctuations or reference voltage modulations in variety of situations like DVS systems with reconfigurable converters
- Improvement on voltage drop characteristics of an on chip distributed voltage converter
- Improvement on hardware security against power side channel attacks

In summary, i) improvement of transient response reduces the power losses in a DVS system and keeps the power supply noise low while benefiting from reduced parasitics between the control system and the load, ii) increased voltage drop of the power grid at different portions of the circuit causes performance to drop since the maximum achievable clock frequency is limited by the slowest section and can be improved only by using an over designed or a fully integrated power delivery system, iii)

hiding the power trace of the load circuit behind an integrated voltage converter prevents attackers from committing side channel attacks without sensing signals inside the chip.

The converter gating method is introduced in the Chapter 2. The converter gating uses a number of smaller converter stages that are adaptively turned on or off based on the workload to maintain high efficiency over wide range of output currents. The power efficiency benefits of this control method is verified with analysis and simulations. Since the losses do not scale perfectly for smaller output power levels, using converter gating results in 5-12 % increased efficiency at lower output currents. The response speed of the converter gating technique is improved through using an additional operational state where the converter operates at a different conversion ratio to boost the charge transferred to the output, reducing the transient settling time from 1.4 us to 104 ns. Furthermore, the proposed method has each phase of the voltage converter distributed throughout the power grid which provide closer to load regulation negating the effects of the power grid on the power supply integrity. The activation pattern of separate stages are also randomized to reduce the correlation of the input power and the load current profile to increase hardware security. Activation pattern causes 20 ns of timing uncertainty that changes the input power waveform for the same load pattern.

This work extends the previously known analysis methods to cover the transient response characteristics of switched capacitor voltage converters to provide a foundation for the methods to improve the transient response in Chapter 3. First, the operation of SC voltage converters in general is analyzed, then the mathematical equations for the 1/1 converters are derived. As pointed out in Chapter 3, the results from 1/1 converter can be extended to characterize all other configurations since the converters show similar behavior even with different configurations and the results from 1/1 converter can be scaled to fit other conversion ratios. The results are then used to analyze the charge transfer rates in reconfigurable converters with more than 1 conversion ratios. Analysis showed that the charge transfer rate experiences sudden increases or drops during reconfiguration which affects the transient behavior during reconfiguration. Moreover, it is found that some of the transient enhancement methods described in the literature also suffer from the same type of change in charge transfer rates under specific circumstances. In the analysis the control loop and

the integrator is found to be the source of the unexpected behavior during response. An alternative method of adaptive gain modification is proposed to mitigate the transient response issues and provide fast response to transients on either load power or reference voltage. This improvement is achieved by modifying the gain of the integrator in the control loop depending on the difference between the output voltage and the target voltage and creating a fast recovery state in either direction of the load current step or the voltage reference step. These improvements are verified using simulations and experimental results will be completed in the future.

Finally to confirm the theoretical assumptions and simulation results a prototype circuit is designed and explained in Chapter 4. The design focuses on fast transient response using method proposed in Chapter 3, while also providing high power density and high efficiency over wide output power range. The design is sent for fabrication in 28 nm FDSOI technology. The target parameters for the design are 1.6 to 2.2 V input voltage range, 0.6 to 0.9 V output voltage range and 0 to 200 mA output current. At the highest efficiency of 75% the design is expected to deliver approximately 750 mW/mm^2, and is expected to maintain over 70% efficiency for most of the output current range. The security improvements could not be implemented on the same design as a separate control method would have been necessary.

5.1 Future Work

In the future, the measurements for the test chip will be completed to prove the operation of the proposed method. These measurements will include the DC performance characteristics and the transient characteristics.

The simulations provided in Chapter 3 will be verified experimentally. This can be done using a converter with 1/2 and 1/1 conversion ratios, and can be done using a discrete solution on a PCB.

The analysis provided in Chapter 3, offers a very simple approach to analyzing different conversion ratios and the charge transfer in general. The simplified analysis, may help in creating linear system models for SC DC-DC converters which will be useful in analyzing the behavior of control loops with precision. More importantly, if these models are extended to cover the output

voltage ripple characteristics, the ripple can also be controlled within a loop to prevent spurs at selected frequencies. This may help with the applications where the output voltage ripple is not limited by the sensitivity of the load circuit, rather it is limited by the electromagnetic interference it creates.

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APPENDICES

Appendix A: Verilog Code for Control Logic

```
module top(
reset,
clk,
clk_gain,
internal_comp_superhigh,
internal_comp_high,
internal_comp_low,
internal_comp_superlow,
external_comp_superhigh,
external_comp_high,
external_comp_low,
external_comp_superlow,
en_comp_bypass,
integration,
outputther
);

output [1023 : 0] outputther;
output [9:0] integration;
wire [1023 : 0] outputther;

input reset;
input clk;
input clk_gain;
input internal_comp_superhigh;
input internal_comp_high;
```

Appendix A (Continued)

```
input internal_comp_low;
input internal_comp_superlow;
input external_comp_superhigh;
input external_comp_high;
input external_comp_low;
input external_comp_superlow;
input en_comp_bypass;

integrator i1 (
.reset(reset),
.clk(clk),
.clk_gain(clk_gain),
.internal_comp_superhigh(internal_comp_superhigh),
.internal_comp_high(internal_comp_high),
.internal_comp_low(internal_comp_low),
.internal_comp_superlow(internal_comp_superlow),
.external_comp_superhigh(external_comp_superhigh),
.external_comp_high(external_comp_high),
.external_comp_low(external_comp_low),
.external_comp_superlow(external_comp_superlow),
.en_comp_bypass(en_comp_bypass),
.integration(integration)
);

bintother bintother_1 (
.inputbin(integration),
```

Appendix A (Continued)

```
.outputther(outputther)
);

endmodule

module integrator(
reset,
clk,
clk_gain,
internal_comp_superhigh,
internal_comp_high,
internal_comp_low,
internal_comp_superlow,
external_comp_superhigh,
external_comp_high,
external_comp_low,
external_comp_superlow,
en_comp_bypass,
integration);

output [9 : 0] integration;
reg [9 : 0] integration;

input clk;
input reset;
input clk_gain;
```

Appendix A (Continued)

```
input internal_comp_superhigh;
input internal_comp_high;
input internal_comp_low;
input internal_comp_superlow;
input external_comp_superhigh;
input external_comp_high;
input external_comp_low;
input external_comp_superlow;
input en_comp_bypass;

reg [5:0] gain_counter;
wire [3:0] comp_signal;

assign comp_signal = (en_comp_bypass) ? {external_comp_superhigh,
   external_comp_high, external_comp_low, external_comp_superlow} : {
   internal_comp_superhigh, internal_comp_high, internal_comp_low,
   internal_comp_superlow};

always @(posedge clk_gain or negedge reset) begin
if(!reset) begin
gain_counter <= 1;
end //End reset
else begin
gain_counter <= gain_counter + 1;
end
end
```

Appendix A (Continued)

```
always @(posedge clk or negedge reset) begin
if(!reset) begin
integration <= 1023;
end //End reset

else begin
case(comp_signal)
0: begin
if( integration <= 1023 - gain_counter ) begin
integration <= integration + gain_counter;
end
else begin
integration <= 1023;
end
end //End condition 1

1: begin
if( integration < 1023 ) begin
integration <= integration + 1;
end
else begin
integration <= 1023;
end
end //End condition 2
```

Appendix A (Continued)

```
3: begin
integration <= integration;
end //End conditon 3

7: begin
if( integration > 0 ) begin
integration <= integration - 1;
end
else begin
integration <= 0;
end
end //End condition 4

15: begin
if( integration >= gain_counter ) begin
integration <= integration - gain_counter;
end
else begin
integration <= 0;
end
end //End condition 5

default: begin
integration <= integration;
end
endcase
```

Appendix A (Continued)

```
end //End main block
end

endmodule

module bintother(
inputbin,
outputther
);

input  [9:0]            inputbin;
output [1023:0]         outputther;

generate
genvar i;
for(i=0; i<1024; i=i+1) begin : foo
assign outputther[i] = (inputbin >= i) ? 1 : 0;
end
endgenerate

endmodule
```

Appendix B: Copyright Notices

The following notice is for the material in Chapter 2.

Appendix B (Continued)

The following notice is for the material in Chapter 2.

ABOUT THE AUTHOR

Orhun Aras Uzun received the B.Sc. degree in Electronics Engineering from Istanbul Technical University in 2012. He is currently working for Ph.D. degree at University of South Florida. His main research interest is analog mixed signal integrated circuit design, specifically integrated power management circuits and data converters.